FILE 'HCAPLUS, WPIX,
L1 0 S TW90110699/PN
L2 0 S TW2001-90110699/AP,PRN

FILE 'REGISTRY'
L3 8 S AL2O3/MF
L4 118 S AL.O/MF
L5 3 S O3Y2/MF
L6 63 S O.Y/MF
L7 26 S O.SI.ZR/MF
L8 0 S O.SI.HF/MF
L9 0 S O.HF.SI/MF
L10 6 S HF.O.SI/MF
L11 0 S O3LA2/MF
L12 4 S LA2O3/MF
L13 21 S LA.O/MF
L14 14 S O2ZR/MF
L15 108 S O.ZR/MF
L16 4 S HFO2/MF
L17 24 S HF.O/MF
L18 3 S O5TA2/MF
L19 104 S O.TA/MF
L20 1 S O3PR2/MF
L21 53 S O.PR/MF
L22 17 S O2TI/MF
L23 273 S O.TI/MF
L24 0 S SIO2/MF
L25 48 S O2SI/MF
L26 0 S O2.SI/MF
L27 316 S O.SI/MF

FILE 'HCAPLUS'
L28 1123 S FLASH(W)(MEMORY OR RAM)
L29 14 S G06F-003/06/IC
L30 383510 S L1 OR L2 OR ALUMINATE OR (ALUMINUM OR AL)(W)(OXIDE OR O) OR AL2O3 OR RUBY OR SAPPHIRE OR LEUCOSAPPHIR
E
L31 383510 S ALUMINATE OR (ALUMINUM OR AL)(W)(OXIDE OR O) OR AL2O3 OR RUBY OR SAPPHIRE OR LEUCOSAPPHIRE
L32 87489 S Y2O3 OR (Y OR YTTRIUM)(W)(OXIDE OR O) OR DIYTTRIUM(W)TRIOXIDE OR NANOTEK OR YTTRIUM(W)SESQUIOXIDE
L33 473 S ZRSI(W)O OR SILICON(W)ZIRCONIUM(W)OXIDE
L34 1001 S HFSI(W)O OR HAFNIUM(W)SILICON(W)OXIDE OR HAFNIUM(W)ALLOY

L35 24282 S LA2O3 OR (LA OR LANTHANUM)(W)(OXIDE OR O) OR (DILANTHANUM OR LANTHANUM)(W)(OXIDE OR TRIOXIDE)
L36 84243 S ZRO2 OR (ZR OR ZIRCONIUM)(W)(OXIDE OR O) OR SUPEROXIDO(W)(ZIRCONIUM OR ZR) OR BADDELEYITE
L37 5737 S HFO2 OR (HF OR HAFNIUM)(W)(OXIDE OR O OR DIOXIDE) OR HAFNOTRAST
L38 20480 S TA2O5 OR (TA OR TANTALUM OR DITANTALUM)(W)(OXIDE OR O OR PENTAOXIDE OR PENTOXIDE) OR TANTALIC(W)ACID OR TANTITE
L39 7534 S PR2O3 OR (PRASEODYMIUM OR PR)(W)(OXIDE OR O OR SESQUIOXIDE OR TRIOXIDE) OR PRASEODYMIA
L40 178342 S TIO2 OR (TI OR TITANIUM)(W)(OXIDE OR O) OR RUTILE OR SAGENITE OCTAHEDRITE
L41 397 S SAGENITE OR OCTAHEDRITE
L42 711203 S SIO2 OR (SILICON OR SI)(W)(DIOXIDE OR O2) OR SILICA OR MYRICKITE OR TRIDYMITE OR BOBKOVITE OR MOGANITE OR QUARTZ OR CRISTOBALITE OR ADELITE OR ACTICEL
L43 2490 S ACEMATT OR STISHOVITE OR COESITE OR SIBELITE OR CRYSVARL OR CRYSTOBALITE OR SARDONYX OR QUARTZINE OR SIKRON OR MILLISIL OR ROCK(W)CRYSTAL
L44 1137 S (L28 OR L29) AND ((L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23 OR L24 OR L25 OR L26 OR L27) OR (L28 OR L29 OR L30 OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41 OR L42 OR L43))
L45 573 S (L28 OR L29) AND ((L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23 OR L24 OR L25 OR L26 OR L27))
L46 586 S (L28 OR L29) AND ((L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23 OR L24 OR L25 OR L26 OR L27) OR (L30 OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41 OR L42 OR L43))
L47 13 S L46 AND (MOUNT? OR STACK? OR PILE?)(3A)(LAY ER? OR FILM OR COAT?)
L48 0 S L46 AND BAND(W)GAP
L49 1137 S (L28 OR L29) AND ((L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23) OR (L28 OR L29 OR L30 OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41))

L50 22 S (L28 OR L29) AND ((L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23) OR (L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41))

L51 346 S L46 AND (DIELECTRIC OR OXIDE OR INSULAT?)(3A)(FILM OR LAYER? OR COAT?)

L52 285 S L51 AND GATE

L53 182 S L51 AND FLOAT?(2A)GATE

L54 103 S L52 AND (SOURCE AND DRAIN)

L55 69 S L53 AND (SOURCE AND DRAIN)

L56 98 S L53 AND (TUNNEL? OR TRENCH? OR GROOV?)

L57 28 S L56 AND(STACK? OR MOUNT?)

L58 110 S L47 OR L50 OR L55 OR L57

L59 110 DUP REMOVE L58 (0 DUPLICATES REMOVED)
SEL PN

L60 110 S (US5970342/PN OR EP718895/PN OR EP1005081/PN OR TW428319/PN OR US2002086521/PN OR US2002086555/PN OR US2002160571/PN OR US2002160575/PN OR US5998264/PN OR US6008090
/PN OR US6117731/PN OR CN1239325/PN OR EP1074046/PN OR JP08227944/PN OR JP08330452/PN OR JP09082674/PN OR JP09307083/PN OR JP10084052/PN OR JP10093057/PN OR JP10189921/PN OR JP11297867/PN OR JP11354655/PN OR JP2000049243/PN OR JP2000164834/PN OR JP2000260887/PN OR JP2001127260/PN OR JP2001168218/PN OR JP20020014656/PN OR JP2002026151/PN OR JP2002134634/PN OR JP2002151609/PN OR JP2002246569/PN OR JP2002512450/PN OR "JP2960377 B2"/PN OR "JP3274785 B2"/PN OR "JP3298509 B2"/PN OR "JP3314807 B2"/PN OR KR2000006121/PN OR KR2000044947/PN OR KR9615936/PN OR SG71836/PN OR SG87938/PN OR TW383468/PN OR TW386312/PN OR TW388131/PN OR TW401593/PN OR TW404058/PN OR TW406420/PN OR TW407380/PN OR TW407381/PN OR TW418509/PN OR TW432512/PN OR TW448576/PN OR TW457597/PN OR US2001003366/PN OR US2001012661/PN OR US2001015455/PN OR US2001046738/PN OR US2002000602/PN OR US2002009853/PN OR US2002033500/PN OR US2002033502/PN OR US2002052073/PN OR US2002052079/PN OR US2002055217/PN OR US2002063276/PN OR US2002086548/PN OR US2002086556/PN OR US2002109163/PN OR US2002109167/PN OR US2002110983/PN OR US2002117709/PN OR US2002130357/PN OR US2002137271/PN OR US2002151136/PN OR US2002160570/PN OR US2002167041/PN OR US2002173107/PN OR US5414287/PN OR US5432112
/PN OR US5460988/PN OR US5576232/PN OR US5631179/PN OR US5675162/PN OR US5679591/PN OR US5714412/PN OR US5721442/PN OR US5796142/PN OR US5814862/PN OR US5834806/PN OR US5844270/PN

OR US5851881/PN OR US5877523/PN OR US5885868/PN OR US5923056/P
N OR US5932910/PN OR US5960284/PN OR US5970341/PN OR US5972752/
PN OR US5977584/PN OR US5981341/PN OR US5981358/PN OR US5994185
/PN OR US6011288/PN OR US6011289/PN OR US6037223/PN OR US6048766/PN OR US6051467/PN OR US6057193/PN OR US6060741/PN OR US6066874/PN OR US6078076/PN OR US6084262/P

L61 6 S (HSIEH, JUNG-YU OR HSIEH JUNG-YU OR HSIEH, J Y OR HSIEH J Y)/AU

L62 0 S (HSIEH, JUNG YU OR HSIEH JUNG YU)/AU

L63 511 S (LIN C H OR LIN, C H OR LIN CHIN HSIANG OR LIN, CHIN HSIANG)/AU

L64 38 S (L61 OR L63) AND ((L30 OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41) OR (L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23))

L65 0 S L64 AND (L28 OR L29)

FILE 'WPIX, JAPIO'

L66 131 S L60

L67 556 S T01-C01C/MC

L68 22 S (L67 OR L28 OR L29) AND ((L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38 OR L39 OR L40 OR L41))

L59 ANSWER 1 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:869365 HCAPLUS
DN 137:344892
TI Method of forming **flash memories** with high coupling ratio and the structure of the same
IN Tseng, Horng-Huei
PA Taiwan
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002167041	A1	20021114	US 2001-852405	20010509

AB The **flash memory** structure includes a substrate having **trenches** formed therein, a 1st **dielec. layer** and a 1st conductive **layer** are **stacked** on the substrate. Isolations are formed in the **trenches** and protruding over the surface of the substrate, wherein the 1st conductive layer is also protruded over the isolations. A 2nd conductive layer is lying the surface of the 1st conductive **layer** and a 2nd **dielec. layer** formed thereon. A 3rd conductive layer is formed on the 2nd **dielec. layer**. The **floating gate** is consisted of 1st conductive layer and the 2nd conductive layer.

L59 ANSWER 2 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:833451 HCAPLUS
DN 137:331953
TI High coupling ratio **stacked**-gate **flash memory** integrated circuit and fabrication thereof
IN Tseng, Horng-Huei
PA Taiwan
SO U.S. Pat. Appl. Publ., 5 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002160575	A1	20021031	US 2001-846468	20010430
US 2002160571	A1	20021031	US 2001-976446	20011012
PRAI US 2001-846468	A2	20010430		

AB The invention relates to a **stacked**-gate **flash memory** cell comprising a **trench** formed in a substrate and a **tunneling** oxide is formed on the substrate. A first part of the **floating gate** is formed on the **tunneling dielec. layer**. A protruding isolation filler is formed in the **trench** and protruding over the upper surface of the first part of the **floating gate**, thereby forming a cavity between the two adjacent raised isolation filler. A second part of the **floating gate** is formed along the surface of the cavity to have a U-shaped structure in cross sectional view. A **dielec. layer** is conformally formed on the surface of the second part of the **floating gate** and a control gate is formed on the **dielec. layer**.

L59 ANSWER 3 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:833447 HCAPLUS
DN 137:331949

12/05/2002

TI STI in **stacked**-gate **flash memory** integrated circuit and fabrication thereof
IN Tseng, Horng-Huei
PA Taiwan
SO U.S. Pat. Appl. Publ., 7 pp., Cont.-in-part of U.S. Ser. No. 846,468.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002160571	A1	20021031	US 2001-976446	20011012
US 2002160575	A1	20021031	US 2001-846468	20010430
PRAI US 2001-846468	A2	20010430		

AB The invention relates to q **stacked**-gate **flash memory** cell comprising a **trench** formed in a substrate and a **tunneling** oxide is formed on the substrate. A first part of the **floating gate** is formed on the **tunneling dielec. layer.** A protruding isolation filler is formed in the **trench** and protruding over the upper surface of the first part of the **floating gate,** thereby forming a cavity between the two adjacent raised isolation filler. A second part of the **floating gate** formed of HSG-Si is formed along the surface of the cavity to have a U-shaped structure in cross sectional view. A **dielec. layer** is conformally formed on the surface of the second part of the **floating gate** and a control gate is formed on the **dielec. layer.**

L59 ANSWER 4 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:833446 HCAPLUS
DN 137:331948
TI **Stacked**-gate **flash memory** and the method of making the same
IN Tseng, Horng-Huei
PA Taiwan
SO U.S. Pat. Appl. Publ., 5 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002160570	A1	20021031	US 2001-846470	20010430

AB A method for manufg. a **flash memory** comprises forming a first **dielec. layer** on a semiconductor substrate as a **tunneling** dielec. and forming a first conductive **layer** on the first **dielec. layer.** Next step is to pattern the first **dielec. layer,** the first conductive layer and the substrate to form a **trench** in the substrate. An isolation is refilled into the **trench,** a portion of isolation is removed to a surface of the first conductive layer. A portion of the first conductive layer is removed, thereby forming a cavity between adjacent isolation. A second conductive layer is formed along a surface of the cavity and the isolation, next, a portion of the second conductive layer is removed to a surface of the isolation. Subsequently, a second **dielec. layer** is formed on a surface of the **floating gate,** a third conductive layer is formed on the second **dielec. layer** as a control gate.

L59 ANSWER 5 OF 110 HCAPLUS COPYRIGHT 2002 ACS

12/05/2002

AN 2002:716768 HCAPLUS
DN 137:240747
TI Self-aligned **floating gate** flash cell system and method
IN Hurley, Kelly T.; Wolstenholme, Graham
PA USA
SO U.S. Pat. Appl. Publ., 25 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002130357	A1	20020919	US 2001-808484	20010314

AB Methods and devices are disclosed using a polysilicon wings or ears in a **stacked** gate region. The **stacked** gate region includes a substrate, at least one **trench**, an **oxide layer**, at least one **floating gate** layer and at least one polysilicon wing. The substrate has at least one semiconductor layer. The at least one **trench** is formed in the substrate and filled with an oxide. The **oxide layer** is formed over the substrate and the **trench**. The at least one **floating gate** layer is formed over the **oxide layer**. The at least one polysilicon wing is formed adjacent to vertical edges of the at least one **floating gate layer** and over the **oxide layer**. The present invention includes polysilicon wings or ears which can increase the capacitive coupling of memory cells in memory devices in which they were used. Generally, the polysilicon wings or ears are placed proximate to the **floating gate** of a memory cell. Thus, the present invention may allow for further reducing or scaling the size of memory cells and devices.

L59 ANSWER 6 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:616305 HCAPLUS
DN 137:178114
TI Method of fabricating a split-gate **flash memory** cell
IN Liu, Chih-cheng; Wu, De-yuan
PA Taiwan
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002110983	A1	20020815	US 2001-779487	20010209

AB The invention relates to a process for making a split gate **flash memory** cell. Firstly, a cap layer is formed on the surface of a silicon base of the semiconductor wafer. The surface of the silicon base is then etched to form at least one shallow trench. The shallow trench comprises a vertical sidewall composed of a portion of the silicon base. Next, an ion implantation process is performed using the cap layer to as a mask in order to form a doped area in both the bottom surface of the shallow trench and the silicon base beneath the cap layer. The doped area functions as a **source**. A first **dielec. layer**, **floating gate**, second **dielec. layer**, and a control gate are formed, resp., the width of the **floating gate** being shorter than the width of the first **dielec. layer**. Then, a third **dielec. layer** is formed on the control gate and the cap layer is removed. Finally, an elec. conduction layer is formed on the surface of the silicon

base to function as a **drain** to complete the split gate **flash memory** cell of the present invention.

L59 ANSWER 7 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:616095 HCAPLUS
DN 137:162428
TI Memory device and method of fabrication thereof
IN Kang, Chang Yong; Kim, Young Gwan
PA S. Korea
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002109167	A1	20020815	US 2001-33013	20011227
	JP 2002246569	A2	20020830	JP 2001-397230	20011227
PRAI	KR 2000-83819	A	20001228		

AB In order to improve an operation property of a magnetic RAM (MRAM) having a higher speed than an SRAM, integration as high as a DRAM, and a property of a nonvolatile memory such as a **flash memory**, an oxide film is thinly formed on a 2nd word line which is a write line, and an magnetic tunnel junction (MTJ) cell is formed according to a succeeding process. The MRAM is formed by reducing a distance between the write line and the MTJ cell. It is possible to perform a write operation with a small current.

L59 ANSWER 8 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:505384 HCAPLUS
DN 137:71469
TI Methods of forming silicon-doped **aluminum oxide**, and methods of forming transistors and memory devices
IN Ahn, Kie Y.; Forbes, Leonard
PA Micron Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 11 pp., Division of U.S. Ser. No. 754,926.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002086555	A1	20020704	US 2001-12619	20011105
	US 2002086521	A1	20020704	US 2001-754926	20010104
PRAI	US 2001-754926	A3	20010104		

AB The invention encompasses a method of forming a silicon-doped **aluminum oxide**. **Aluminum oxide** and silicon monoxide are coevapd. Subsequently, at least some of the evapd. **aluminum oxide** and silicon monoxide is deposited on a substrate to form the silicon-doped **aluminum oxide** on the substrate. The invention also encompasses methods of forming transistors and **flash memory** devices.

L59 ANSWER 9 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:505378 HCAPLUS
DN 137:71465
TI Method for forming gate dielectric layer in NROM
IN Chang, Kent Kuohua
PA Taiwan
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO

DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002086548	A1	20020704	US 2000-735894	20001214

AB The invention relates to a process for making a gate dielec. layer in nitride read only memory (NROM) device, wherein the tunnel oxide layer consists of a **zirconium oxide** layer. **Zirconium oxide** layer can increase coupling ratio of gate dielec. layer and reliability for nitride read only memory type **flash memory** is improved. This invention, a substrate is provided and a **zirconium oxide** layer is formed on substrate by reactive magnetron sputtering and a silicon nitride layer is sandwiched between a **zirconium oxide** layer and a silicon oxide layer. Then, an ONO layer (oxide-nitride-oxide layer) is formed. The method is using **zirconium oxide** as gate dielec. can reduce leakage current, increase drain current, improve subthreshold characteristics, and electron and hole mobilities.

L59 ANSWER 10 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:505366 HCAPLUS
DN 137:71453
TI Methods of forming silicon-doped **aluminum oxide**, and methods of forming transistors and memory devices
IN Ahn, Kie Y.; Forbes, Leonard
PA USA
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002086521	A1	20020704	US 2001-754926	20010104
US 2002086555	A1	20020704	US 2001-12619	20011105
US 2002086556	A1	20020704	US 2001-12677	20011105
PRAI US 2001-754926	A3	20010104		

AB The invention encompasses a method of forming a silicon-doped **aluminum oxide**. **Aluminum oxide** and silicon monoxide are co-evapd. Subsequently, at least some of the evapd. **aluminum oxide** and silicon monoxide is deposited on a substrate to form the silicon-doped **aluminum oxide** on the substrate. The invention also encompasses methods of forming transistors and **flash memory** devices.

L59 ANSWER 11 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:354042 HCAPLUS
DN 136:362636
TI Semiconductor device with a self-aligned trench isolation
IN Kanamori, Kohji
PA Japan
SO U.S. Pat. Appl. Publ., 22 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002055217	A1	20020509	US 2001-32764	20011022
JP 2002134634	A2	20020510	JP 2000-325656	20001025

PRAI JP 2000-325656 A 20001025

AB The present invention relates generally to a semiconductor device having element isolation using a trench that can be self-aligned with a **stacked film** pattern formed in a cell. A semiconductor device including memory cells isolated by a trench that may be self aligned with a **stacked film** pattern has been disclosed. The memory cells may be **flash memory** cells having an active gate film that may be thinner than a gate oxide film. The active gate film may be located in a central portion under of a gate electrode. The gate oxide film may be located under end portions of the gate electrode. In this way, a distance between a shoulder portion of a trench and a gate electrode may be increased. Thus, an elec. field concn. in the shoulder portion of the trench may be decreased and memory cell characteristics may be improved.

L59 ANSWER 12 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:332640 HCAPLUS
DN 136:362506
TI Memory cell structure of **flash memory** having circumventing **floating gate** and method for fabricating the same
IN Wen, Wen Ying
PA Taiwan
SO U.S. Pat. Appl. Publ., 12 pp., Cont.-in-part of U.S. Ser. No. 653,319.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002052079	A1	20020502	US 2001-948675	20010910
PRAI	US 2000-653319	A2	20000901		

AB The present invention relates to a memory cell structure of a **flash memory** and a method for fabricating the same and, more particularly, to a **flash memory** having circumventing **floating gates** and a method for fabricating the same. In the proposed memory cell, a **floating gate** and a tunneling oxide are etched to form an annular shape situated between a **drain**, a **source**, and 2 field oxides. An interpoly dielec. and a control gate cover in turn on the **floating gate** and on the surface of the substrate not covered by the **floating gate** by means of self-alignment. The present invention can not only achieve self-alignment to form the control gate and apply to high-integration memory cells with small areas, but also can effectively increase the high capacitance coupling ratio thereof to enhance the tunneling effect of hot electrons.

L59 ANSWER 13 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:221070 HCAPLUS
DN 136:255738
TI Method for manufacturing low voltage **flash memory**
IN Shin, Jung-wook; Kim, Jae-seung; Kim, Hong-seub
PA Anam Semiconductor, Inc., S. Korea
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002033502	A1	20020321	US 2001-947419	20010905

PRAI KR 2000-52260 A 20000905
AB A memory comprises a gate **oxide layer** formed on a semiconductor substrate; an ion trap region formed in a corner portion of the gate **oxide layer**; a **floating gate** formed on the gate **oxide layer**; a **dielec. layer** formed on the **floating gate**; a control gate formed on the **dielec. layer** ; a spacer provided along side walls of a formed gate; an LDD formed under the spacer on the semiconductor substrate, the LDD being doped at a low concn. with impurities; and a **source/drain** region formed on an element region of the semiconductor substrate contacting the LDD, the **source/drain** region being doped at a high concn. with impurities. The ion trap region is formed by performing ion injection into a corner portion of the gate oxide after the gate, including the control **gate** and the **floating gate**, is formed.

L59 ANSWER 14 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:72771 HCAPLUS
DN 136:127696
TI Method of manufacturing **flash memory** device
IN Cho, Byung Hee; Kwak, Noh Yeal
PA S. Korea
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002009853	A1	20020124	US 2001-875734	20010606
	US 6472273	B2	20021029		
PRAI	KR 2000-37002	A	20000630		

AB A method of manufg. a **flash memory** device includes the steps of sequentially forming a tunnel **oxide film** and a first polysilicon layer on a semiconductor substrate in which a device sepn. film is formed and then patterning the tunnel **oxide film** and the first polysilicon layer to form a **floating gate**; forming a mask so that a portion in which a **source** region will be formed can be exposed and then removing the device sepn. film at the exposed portion; forming a **dielec. film** including a lower **oxide film**, a nitride **film** , and an upper **oxide film** on the entire structure; performing an annealing process; then forming a second polysilicon **layer** on the **dielec. film**; sequentially removing the polysilicon **layer**, the upper **oxide film**, and the nitride film in a portion in which a **source** region and a **drain** region will be formed, and injecting impurity ions into the semiconductor substrate at a portion in which the lower **oxide film** remains to form a **source** region and a **drain** region; after removing the remaining lower **oxide film**, sequentially forming a third polysilicon layer and a tungsten silicide layer on the entire structure and then patterning the third polysilicon layer and the tungsten silicide layer to form a control gate; and performing an annealing process for activating the impurity ions injected into the **source** region and the **drain** region.

L59 ANSWER 15 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:10931 HCAPLUS
DN 136:78292
TI V-shaped **flash memory** structure

IN Lee, Robin
PA Taiwan
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002000602	A1	20020103	US 2000-538995	20000330
	TW 448576	B	20010801	TW 2000-89105151	20000321
	US 6372564	B1	20020416	US 2000-538998	20000330
PRAI	TW 2000-89105151	A	20000321		

AB A **flash memory** having a V-shaped **stack** gate structure. The V-shaped **stack** gate is formed by implanting ions into a substrate to form a buried **source** line using a mask, and then forming a V-shaped **trench** that exposes the buried **source** line in the substrate. A V-shaped word line **stack** gate is next formed over the **trench** and the substrate next to the **trench**. A common **drain** terminal is formed in the substrate on each side of the V-shaped **stack** gate. The **drain** terminal is elec. connected to a bit line by forming a contact plug.

L59 ANSWER 16 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:845524 HCAPLUS
DN 137:331986
TI Method for fabricating self-aligned gate of **flash memory** cell
IN Kim, Hyeon-Seag
PA Advanced Micro Devices, Inc., USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6475863	B1	20021105	US 2002-150556	20020517

AB For fabricating a **flash memory** cell beyond photolithog. restrictions and with min. bit line leakage current and max. area of **drain** and **source** bit-line silicides, a dummy gate structure is formed on an active device area of a semiconductor substrate. A **drain** bit line junction is formed within the active device area of the semiconductor substrate to a 1st side of the dummy gate structure, and a **source** bit line junction is formed within the active device area of the semiconductor substrate to a 2nd side of the dummy gate structure. A **drain** bit line silicide is formed within the **drain** bit line junction, and a **source** bit line silicide is formed within the **source** bit line junction. Also, an interlevel material is formed to surround the dummy gate structure, and the dummy gate structure is then etched away to form a gate opening within the interlevel material. Spacers are then formed at sidewalls of the gate opening within the gate opening. After formation of the spacers, a tunnel dielec. structure is formed at a bottom wall of the gate opening, and a **floating gate** structure is formed on the tunnel dielec. structure within the gate opening. A floating dielec. structure is formed on the **floating gate** structure within the gate opening, and a control gate structure is formed on the floating dielec. structure within the gate opening. In this manner, a self-aligned gate structure is formed to be comprised of the

tunnel dielec. structure, the **floating gate** structure, the **floating** dielec. structure, and the control gate structure between the spacers within the gate opening.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 17 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:808391 HCAPLUS
DN 137:318986
TI High capacitive-coupling ratio of **stacked**-gate **flash memory** having high mechanical strength **floating gate**
IN Tseng, Horng-Huei
PA Vanguard International Semiconductor Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6468862	B1	20021022	US 2001-990156	20011120

AB A simple and effective method is given for reducing the size of a nonvolatile **flash memory** structure in order to increase the degree of integration. A structure of a **stacked** gate of a **flash memory** cell and a method for forming the same is disclosed. A semiconductor substrate having a 1st conductive gate structure, wherein the 1st gate conductive structure is disposed in between two neighboring raised shallow **trench** isolation structures, the dielec. pillar disposed on the sidewall of the 1st gate conductive structure having a top surface level higher than a top surface of the 1st gate conductive structure, formed thereon. A conformal conductive layer is formed over the said structure. The conductive layer is patterned to form a 2nd gate conductive structure. The 1st and the 2nd gate conductive structures forms a **floating gate**. Next, a thin **dielec. layer** is formed over the **floating gate** structure, then another conductive layer is formed over the **dielec. layer**, and the said conductive layer is patterned to form a control gate.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 18 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:790270 HCAPLUS
DN 137:303245
TI Surrounding-gate **flash memory** having a self-aligned control gate
IN Hsieh, Tsong-minn
PA United Microelectronics Corp., Taiwan
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6465838	B1	20021015	US 2000-630868	20000802
	US 2002033500	A1	20020321	US 2001-925337	20010809
PRAI	US 2000-630868	A3	20000802		

AB A surrounding-gate **flash memory** having a greater capacitor area between the control **gate** and the **floating**

gate and a higher coupling ratio for the control gate is claimed. Device isolation structures are located on the substrate. **Sources** are provided on the top layer of the substrate between two device isolation structures. Tunneling **oxide layers** are provided at both ends of the device isolation structures and on the substrate where the **sources** are present. **Drains** are provided in the top layer of the substrate where the tunneling **oxide layer** is absent in between the device isolation structures. Polysilicon blocks are extended across the ends of two device isolating structures, above the tunnel **oxide layer**. A Si **oxide** cap **layer** is located on the polysilicon block. The Si **oxide layers** are formed on the sidewalls of the polysilicon blocks. The polysilicon layer is on the sidewall of the polysilicon blocks and the polysilicon blocks are sepd. by the Si **oxide layer**. The Si **oxide layer** covers the surface of the polysilicon layers. Another polysilicon layer, which is located on the tunnel Si **oxide layer** above the **sources** also, covers a part of the Si **oxide** cap **layer**.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 19 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:790268 HCAPLUS
DN 137:303243
TI Charge gain/charge loss junction leakage prevention for **flash memory** by using double isolation/capping layer between lightly doped drain and gate
IN Pham, Tuan Duc; Ramsbey, Mark T.; Haddad, Sameer S.; Hui, Angela T.
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6465835	B1	20021015	US 2000-487964	20000118
PRAI	US 1999-156462P	P	19990927		

AB A **flash memory** device with low leakage having core stacks and periphery stacks which are protected by 1st and 2nd thin side walls, side spacers over the side walls, and an HTO **layer** over the **stacks**, and side spacer. The **flash memory** device has an intermetallic dielec. layer placed over the HTO layer. A W plug is placed in the intermetallic dielec. layer to provide an elec. connection to the drain of the **flash memory** device. The addnl. 1st and 2nd side walls reduce current leakage between core stacks and the W plug and help to protect the stacks during fabrication.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 20 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:770165 HCAPLUS
DN 137:287520
TI Scalable dual-bit **flash memory** cell and its contactless **flash memory** array
IN Wu, Ching-Yuan
PA Silicon Based Technology Corp., Taiwan
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent

LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6462375	B1	20021008	US 2002-109873	20020401

AB A scalable dual-bit **flash memory** cell of the present invention comprises a scalable gate region having a pair of **floating-gate** structures with a select-gate region being formed therebetween and a planarized control/select-gate over a 2nd gate-**dielec. layer** being formed over the pair of **floating-gate** structures with or without a pair of 2nd sidewall dielec. spacers being formed over a pair of **floating gates**; a conductive bit line together with a 1st sidewall dielec. spacer being formed over a flat bed formed by a **source/drain** diffusion region and etched raised field-**oxide layers**. A contactless dual-bit **flash memory** array of the present invention comprises a plurality of conductive bit-lines being formed transversely to a plurality of parallel STI regions and a plurality of word lines integrated with a plurality of control-gate/select-gates of the described cells being patterned and formed transversely to the plurality of conductive bit-lines.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 21 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:770164 HCAPLUS
DN 137:287519
TI Design and fabrication of a scaled **stack**-gate **flash memory** device
IN Wu, Ching-Yuan
PA Silicon-Based Technology Corp., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6462372	B1	20021008	US 2001-973094	20011009

AB The present invention relates generally to a **stack**-gate **flash memory** device and more particularly to a scaled **stack**-gate **flash memory** device having an integrated **source/drain** landing island acting as a field-emission cathode/anode for erasing and programming without involving the channel region. A **stack**-gate structure including a masking **dielec. layer** over a control-gate layer over an inter-gate **dielec. layer** over a **floating-gate** layer formed on a gate-**dielec. layer** is formed on a semiconductor substrate having an active region isolated by field-oxides and is oxidized to form a 1st **dielec. layer** over the sidewalls of the control-gate **layer**, a 2nd **dielec. layer** over the sidewalls of the **floating-gate layer**, and a thicker **oxide layer** over each side portion of the active region having a graded **oxide layer** formed at .apprx.2 gate edges. An integrated **source/drain** landing island having a portion formed over a **source/drain** diffusion region for contact and an extended portion formed over a 2nd **dielec. layer** and on a graded-**oxide layer** is employed as a field-emission cathode/anode. The scaled **stack**-gate **flash memory** device of the present invention can be

programmed and erased through 2-**tunneling** paths or 1 **tunneling** path without involving the channel region.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 22 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:690196 HCAPLUS
DN 137:225258
TI Capping layer for a **flash memory** device
IN Pham, Tuan Duc; Ramsbey, Mark T.; Haddad, Sameer S.; Hui, Angela T.
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp., Cont. of U.S. Ser. No. 484,858.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6448608	B1	20020910	US 2000-631894	20000804
PRAI	US 1999-156196P	P	19990927		
	US 2000-484858	A1	20000118		

AB An improved **flash memory** device, which comprises core stacks and periphery stacks which are protected with an oxide layer, a protective layer and an insulating layer. A high energy dopant implant is used to pass the dopant through the insulating layer, the protective layer, and oxide layer into the substrate to create source and drain regions, without using a self aligned etch. The **flash memory** device has an intermetallic dielec. layer placed over the core stacks and the periphery stacks. A tungsten plug is placed in the intermetallic dielec. layer to provide an elec. connection to the drain of the **flash memory** device. The use of a high energy dopant implant to pass through dopant through the insulating layer, the protective layer, and the oxide layer into the substrate without the use of a self aligned source etch, reduces damage to the core stacks and periphery stacks caused by various etches during the prodn. of the **flash memory** device and provides insulation to reduce unwanted current leakage between the tungsten plug and the stacks.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 23 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:588944 HCAPLUS
DN 137:133296
TI Parasitic surface transfer transistor cell (PASTT cell) for bi-level and multi-level NAND **flash memory** and its fabrication
IN Doong, Kelvin Yin-Yuh; Hsu, Ching-Hsiang
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 29 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6429081	B1	20020806	US 2001-858530	20010517
	US 2002173107	A1	20021121	US 2002-186529	20020701
PRAI	US 2001-858530	A3	20010517		

AB An effective **flash memory** cell device with a parasitic surface transfer transistor (PASTT) for improved programming speed and data retention and a method of low-cost, easy manuf. are achieved. The device comprises, 1st, a semiconductor substrate. The semiconductor

substrate further comprises an active area and an isolation barrier region. A **source** junction is in the active area. A **drain** junction is in the active area. A cell channel is in the active area extending from the **drain** junction to the **source** junction. A parasitic channel is in the active area on the top surface of the semiconductor substrate extending from the **drain** junction to the **source** junction. The parasitic channel is bounded on one side by the isolation barrier region and on another side by the cell channel. A **floating gate** comprises a 1st conductive layer overlying the cell channel with a tunneling **oxide layer** there between. The **floating gate** does not overlie the parasitic channel. A control gate comprises a 2nd conductive layer overlying the **floating gate** with an interlevel **dielec.** **layer** there between. A parasitic surface transfer-transistor (PASTT) gate comprises the 2nd conductive layer overlying the parasitic channel with the interlevel **dielec.** **layer** there between.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 24 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:551639 HCAPLUS
DN 137:102521
TI **Flash memory** with ultra thin vertical body transistors
IN Forbes, Leonard; Ahn, Kie Y.
PA Micron Technology, Inc., USA
SO U.S., 28 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6424001	B1	20020723	US 2001-780169	20010209
US 2002109163	A1	20020815		
WO 2002065522	A1	20020822	WO 2002-US3131	20020204
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
US 2002137271	A1	20020926	US 2002-152649	20020520
PRAI US 2001-780169	A	20010209		

AB The invention relates to a **flash memory** cell with ultrathin vertical body transistors. The **flash memory** includes an array of memory cells including **floating gate** transistors. Each **floating gate** transistor includes a pillar extending outwardly from a semiconductor substrate. The pillar includes a single cryst. first contact layer and a second contact layer vertically sepd. by an **oxide layer** . A single cryst. vertical transistor is formed along side of the pillar. The single cryst. vertical transistor includes an ultra thin single cryst. vertical body region which separates an ultra thin single cryst. vertical first **source/drain** region and an ultrathin single cryst. vertical second **source/drain** region. A **floating gate** opposes the ultra thin single cryst.

vertical body region, and a control gate sepd. from the **floating gate** by an **insulator layer**.
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 25 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:551557 HCAPLUS
DN 137:102491
TI Use of DARC and BARC in **flash memory** processing
IN Holscher, Richard D.
PA Micron Technology, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6423474	B1	20020723	US 2000-532666	20000321

AB A method of using dielec. antireflective coating (DARC) in conjunction with bottom antireflective coating (BARC) to form an antireflective barrier layer is provided. The antireflective layer conforms to the topog. of the substrate surface and is adapted to function effectively in both annealed and unannealed states. The method of using DARC in combination with BARC also inhibits the nitride **layer** of a gate **stack** to seep into adjacent photoresist layers and adversely affect the compn. of the photoresist.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 26 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:367263 HCAPLUS
DN 136:378634
TI Method of fabricating a stringerless **flash memory**
IN Chen, Chien-Wei
PA Macronix International Co. Ltd., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6387814	B1	20020514	US 2001-682215	20010807

AB A semiconductor substrate is provided. A no. of rows of **layer stacks** are formed on the semiconductor substrate with a shallow trench positioned between two adjacent **layer stacks**. Each **layer stack** is a polysilicon **layer** and a sacrificial layer and has two side walls. Each side wall of the **layer stack** intersects the bottom of the shallow trench at an angle of approx. 90 degrees. A HDPCVD silicon oxide layer is deposited to cover the **layer stacks** and the shallow trenches followed by a planarization process to remove portions of the HDPCVD silicon oxide layer to expose in the sacrificial layer. Then, the sacrificial layer is removed. An insulating layer, a word line layer, and a photoresist layer are formed on the polysilicon layer, resp. The photoresist layer is patterned so as to define a position for forming a word line. A first dry etching process is performed to remove portions of the word line layer not covered by the photoresist layer with a first selectivity of polysilicon to silicon oxide. Following that, a second dry etching process is performed to etch portions of the insulating layer not

covered by the photoresist layer with a second selectivity of polysilicon to silicon oxide. Finally, a third dry etching process is performed to etch the polysilicon layer with a third selectivity of polysilicon to silicon oxide, forming a T-shape side view for the remaining polysilicon layer.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 27 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:309837 HCAPLUS
DN 136:317919
TI Formation of nonvolatile memory device comprised of an array of vertical field effect transistor structures resulting in minimum short channel effects
IN Yu, Allen S.
PA Advanced Micro Devices, Inc., USA
SO U.S., 49 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6376312	B1	20020423	US 2001-817628	20010326

AB For fabrication of a vertical field effect transistor structure for each of an array of **flash memory** cells for a nonvolatile memory device, an opening is etched though top and bottom **layers** of doped **insulating** material and a **layer** of dummy material formed between the bottom and top **layers** of doped **insulating** material. The opening is filled with a semiconductor material to form a semiconductor fill. The layer of dummy material is etched away such that a channel region of the semiconductor fill is exposed. A tunnel gate dielec. is formed on the channel region of the vertical field effect transistor. A **floating gate** electrode material is deposited to abut the tunnel gate dielec. The tunnel gate dielec. and the **floating gate** electrode material are disposed on a plurality of planes of the channel region of the vertical field effect transistor. Dopant diffuses from the top and bottom **layers** of doped **insulating** material into the semiconductor fill to form **drain** and **source** extension junctions. A control gate dielec. material and a control gate electrode material are deposited on any exposed surfaces of the **floating gate** electrode material. The control gate electrode material is patterned to be continuous for a row of the array of **flash memory** cells such that the control gate electrode of each vertical field effect transistor of the row of **flash memory** cells is coupled together to form a word line of the nonvolatile memory device. Also, one of the semiconductor fill or a **drain** or **source** contact structure below the semiconductor fill is patterned to be continuous for a column of the array of **flash memory** cells to form a bit line of the nonvolatile memory device. Such a vertical field effect transistor structure may occupy a smaller area of the semiconductor substrate such that a compact array of **flash memory** cells is formed for the nonvolatile memory device.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 28 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:131519 HCAPLUS
DN 136:176608

TI Use of dilute steam ambient for improvement of **tunnel** oxide quality of flash devices
IN Weimer, Ronald A.; Powell, Don C.; Moore, John T.; McKee, Jeff A.
PA Micron Technology, Inc., USA
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6348380	B1	20020219	US 2000-648699	20000825
	US 2002117709	A1	20020829	US 2001-13322	20011113
PRAI	US 2000-648699	A3	20000825		

AB The present invention provides a **flash memory** integrated circuit and a method for fabricating the same. The method includes etching a gate **stack** that includes an initial **oxide layer** directly in contact with a Si **layer**, defining an **oxide**-Si interface there between. By exposing the etched gate **stack** to elevated temps. and a dil. steam ambient, addnl. oxide material is formed substantially uniformly along the oxide-Si interface. Polysilicon grain boundaries at the interface are thereby passivated after etching. In the preferred embodiment, the interface is formed between a **tunnel** oxide and a **floating gate**, and passivating the grain boundaries reduces erase variability due to enhanced charge transfer along grain boundaries. At the same time, oxide in an upper storage **dielec. layer** (**oxide**-nitride-**oxide** or ONO) is enhanced in the dil. steam oxidn. Thermal budget can be radically conserved by growing thin **oxide layers** on either side of a nitride layer prior to etching, and enhancing the **oxide layers** by dil. steam oxidn. through the exposed sidewall after etching. The thin **oxide layers**, like the initial **tunnel** oxide, serve as diffusion paths to enhance uniform distribution of OH species across the buried interfaces being oxidized.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 29 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:69783 HCAPLUS
DN 136:127607
TI Semiconductor memory devices having **flash memory** cells
IN Kobayashi, Kiyoteru
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002026151	A2	20020125	JP 2000-203897	20000705
	JP 20020014656	A1	20020207	JP 2001-756782	20010110
	US 6426529	B2	20020730	US 2001-756782	20010110
PRAI	JP 2000-203897	A	20000705		

AB The memory cell formed on a p-Si substrate in the title devices comprises a channel region, **source/drain** regions formed across the channel region, a **floating gate** formed over a 1st **oxide film** on the channel region, and a control gate formed over a 2nd **oxide film** on the **floating gate**. The **floating gate** comprises a narrow

1st region and a wider 2nd region to give a T-shaped cross-section provided on the channel region, wherein the height of the 1st region is set so as to maximize the **floating gate** voltage upon impression of control voltage on the control gate. The arrangement of the devices provides **flash memory** cells with increased mobility in writing in the memory cells.

L59 ANSWER 30 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:435443 HCAPLUS
DN 135:27951
TI Semiconductor device, nonvolatile semiconductor storage apparatus using the device and fabrication of same
IN Hayashi, Fumihiko
PA Japan
SO U.S. Pat. Appl. Publ., 19 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001003366	A1	20010614	US 2000-732706	20001211
	JP 2001168218	A2	20010622	JP 1999-352358	19991210
PRAI	JP 1999-352358	A	19991210		

AB A semiconductor device which is operable with a small occupied area, high reliability, and low power consumption, a nonvolatile semiconductor storage app. using the device and a manuf. method of the device. A semiconductor device comprises a first **gate insulating film**, **floating gate**, second **gate insulating film**, and control gate on a semiconductor substrate, and a **source** area and a **drain** area formed in the semiconductor substrate on opposite sides of the **floating gate**, the **floating gate** comprises a first **floating gate** and a second **floating gate** disposed to cover the first **floating gate** , and an isolating gate is formed on the second **floating gate** on the side of the semiconductor substrate, and parallel to the first **floating gate** via an isolating **insulating film**.

L59 ANSWER 31 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:792284 HCAPLUS
DN 135:326135
TI Method of forming high k **tantalum pentoxide** **Ta2O5** instead of ONO **stacked films** to increase coupling ratio and improve reliability for **flash memory** devices
IN Au, Kenneth Wo-wai; Chang, Kent Kuohua; Chi, David
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6309927	B1	20011030	US 1999-263983	19990305
	US 2001046738	A1	20011129		

AB In one embodiment, the present invention relates to a method of forming a **flash memory** cell, involving the steps of forming a tunnel oxide on a substrate; forming a 1st polysilicon layer over the

tunnel oxide; forming an insulating layer over the 1st polysilicon layer, the insulating layer comprising an oxide layer over the 1st polysilicon layer, and a **Ta pentoxide** layer over the oxide layer, in which the **Ta pentoxide** layer is made by CVD at a temp. from .apprx.200.degree. to .apprx.650.degree. using an org. Ta compd. and an O compd., and heating in an N2O atm. at a temp. from .apprx.700.degree. to .apprx.875.degree.; forming a 2nd polysilicon layer over the insulating layer; etching at least the 1st polysilicon layer, the 2nd polysilicon layer and the insulating layer, thereby defining at least one stacked gate structure; and forming a source region and a drain region in the substrate, thereby forming at least one memory cell.

RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 32 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:757871 HCAPLUS
DN 135:281756
TI Low voltage, high-coupling ratio **flash memory** cell fabrication
IN Wang, Ling-Sung
PA Taiwan Semiconductor Manufacturing Corporation, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6303960	B1	20011016	US 1999-437503	19991110
	TW 418509	B	20010111	TW 1999-88108047	19990518
PRAI	TW 1999-88108047	A	19990518		

AB A process for manufg. **flash memories** is disclosed. In one embodiment, a 1st **oxide layer** is deposited over a substrate and then, a 1st polysilicon layer is deposited over the **oxide layer**. When the 1st polysilicon layer is etched and formed, an ONO (**oxide** nitride **oxide**) **layer** is deposited over the 1st polysilicon layer. Then, portions of the ONO layer and the 1st polysilicon layer are removed to form two nitride fences. A tunnel **oxide layer** in a conformal shape is subsequently deposited over said nitride fences, some portions of the 1st **oxide layer**, and said substrate. After depositing of tunnel **oxide layer**, a **floating gate** polysilicon **layer**, a 2nd **oxide layer**, and a 2nd polysilicon layer are deposited. Portions of the 2nd polysilicon **layer**, the 2nd **oxide layer**, the **floating gate layer**, and the tunnel **oxide layer** are, subsequently, removed. Finally, a **drain** well and a **source** well are formed in the substrate.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 33 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:668375 HCAPLUS
DN 135:219714
TI Design and fabrication of a low resistance gate **flash memory**
IN Prall, Kirk D.; Pan, Pai-hung
PA Micron Technology, Inc., USA
SO U.S., 17 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6288419	B1	20010911	US 1999-350687	19990709

AB Floating gate stacks are presented having a metal control gate and a polysilicon floating gate and their methods of fabrication that are particularly useful for floating gate memory cells and app. produced therefrom. The metal control gate permits reduced gate resistance and gate height over polysilicon or silicide control gates. An oxidn. barrier is formed on sidewalls of the metal control gate to protect it from oxidn. during oxidn. of sidewalls of the polysilicon floating gate. The oxidn. barrier is useful in reducing peeling, stress and related oxidn. problems when using metals such as W in the metal control gate.

RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 34 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:645651 HCAPLUS
DN 135:203945
TI **Flash memory** cell structure with improved channel punch-through characteristics
IN Ho, Simon Chan Tze; Stodart, Tyrone Philip; Kim, Sung Rae; Lin, Yung-Tao
PA Chartered Semiconductor Manufacturing Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6284603	B1	20010904	US 2000-614555	20000712
SG 87938	A1	20020416	SG 2001-4124	20010711
PRAI US 2000-614555	A	20000712		

AB The invention relates to a method of fabricating semiconductor structures, and more particularly, to a method of fabricating a flash EEPROM device with improved channel punch-through characteristics. Ions are optionally implanted into the semiconductor substrate to form threshold enhancement regions of the same type as the semiconductor substrate. A tunneling oxide is formed. A 1st conductive layer is deposited. An interpoly **oxide layer** is deposited. A 2nd conductive layer is deposited. The 2nd conductive **layer**, the interpoly **oxide layer**, the 1st conductive **layer**, and the tunneling **oxide layer** are patterned to form control **gates** and **floating gates**. Ions are implanted to form **drain** junctions. A mask protects the planned **source** junctions. The **drain** junctions are opposite type to the semiconductor substrate. Ions are implanted to form **source** junctions. A mask protects the **drain** junctions. The **source** junctions are opposite type to the semiconductor substrate. Ions are implanted to form channel stop junctions to complete the flash EEPROM memory cells. The ion implantation is performed at a non-perpendicular angle with respect to the substrate. The channel stop junctions contain the **source** junctions. The channel stop junctions are opposite type to the semiconductor substrate. A mask protects the **drain** junctions.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 35 OF 110 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:569737 HCAPLUS
DN 135:130904
TI Method of manufacturing **flash memory** having a dual **floating gate** structure
IN Chen, Way-ming; Chang, Richard
PA United Microelectronics Corp., Taiwan
SO U.S., 4 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6271089	B1	20010807	US 1999-433955	19991104

AB A method is presented for manufg. a **flash memory** having a dual **floating gate** structure. A **source/drain** region is formed in a substrate. A 1st conductive layer is formed on the substrate and between the **source /drain** region. A 1st **dielec. layer** is located between the substrate and the 1st conductive layer. A **floating gate** mask is formed on the substrate and the 1st conductive layer to expose a portion of the 1st conductive layer. The portion of the 1st conductive layer and a portion of the 1st **dielec. layer** beneath the exposed conductive layer are removed. The **floating gate** mask is removed. A conformal 2nd **dielec. layer** and a 2nd conductive layer are formed over the substrate in sequence. The 2nd conductive **layer** and the 2nd **dielec. layer** are formed to resp. form a control gate and a 3rd **dielec. layer.**
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 36 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:521841 HCAPLUS
DN 135:85644
TI **Flash memory** structure with **stacking** gate formed using damascene-like structure
IN Chen, Jong; Lin, Chrong-jong; Su, Hung-der; Chu, Wen-ting
PA Taiwan Semiconductor Manufacturing Co., Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6261905	B1	20010717	US 2000-560625	20000428

AB A **flash memory** cell and fabrication thereof are disclosed, such that the cell has a damascene-like **stacked** gate. The **stacked** gate is formed not by blanket depositing a 1st polysilicon layer and then subtractively etching to form a **floating gate** followed by the depositing of a 2nd polysilicon layer sepd. by an intervening inter-gate **dielec. layer** over the **floating gate,** but rather a **trench** is formed in a nitride layer formed over a substrate using a modified damascene process. The 1st polysilicon layer is conformally deposited into the damascene-like **trench** to form the **floating gate** of the disclosed cell. Then, a **layer** of inter-gate **dielec. layer** is formed over the 1st polysilicon layer in the **trench,** followed by the forming of a 2nd polysilicon **layer** over the **dielec.**

layer, thus forming the damascene-like **stacked** gate of this invention. The disclosed method alleviates the problem of having poly residues resulting from defects caused by etching the conventionally deposited polysilicon layer. Also, etching over active region can also cause damage to the underlying substrate, which is not the case here. In addn., the method enables the incorporation of the curved structure of the **floating gate** of this invention into the area that increases the coupling ratio of the **flash memory** cell.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 37 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:480740 HCAPLUS
DN 135:69611
TI **Flash memory** structure and method of manufacture which increases the level of integration by reducing the dimensions of the insulator structures
IN Lee, Robin
PA United Microelectronics Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6255689	B1	20010703	US 1999-467251	19991220

AB A **flash memory** cell structure and its method of manuf. The **flash memory** cell has a vertical configuration. An opening and then a trench are formed in a substrate by etching. The trench (defined as the recessed section of the substrate) was used for forming a shallow trench isolation structure. The substrate region between two neighboring openings (defined as the protruding section of the substrate) was used for forming a common **drain** and a channel. A **source** terminal is formed in the substrate at the upper comer next to the shallow trench structure. A tunnel **oxide layer** is formed over the substrate surface of the opening. A **floating gate** and a **dielec. layer** are formed over the tunnel **oxide layer**. A control gate is formed inside the opening.

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 38 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:352249 HCAPLUS
DN 134:335380
TI Design and fabrication of a split gate **flash memory** cell
IN Chen, Chih Ming
PA Taiwan Semiconductor Manufacturing Corporation, Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6232180	B1	20010515	US 1999-347203	19990702

AB A split gate **flash memory** cell formed in a semiconductor substrate is disclosed. The memory cell comprises: a deep n-well formed in the substrate; a p-well formed in the deep n-well; a

select gate structure formed on the p-well, the select gate structure comprising a **stack** of a gate **oxide**, a polysilicon **layer**, and a cap **oxide**; a **tunnel oxide layer** formed on the p-well, the **tunnel** oxide adjacent to the control **gate** structure; a **floating gate** formed over the select gate structure and extending over at least a portion of the **tunnel oxide layer**; a **source** formed in the p-well, the **source** formed adjacent to the **floating gate**; and a **drain** formed in the p-well, the **drain** formed adjacent to the select gate structure. The memory cell is programmed by **source** side channel hot electron and is erased using channel erasing to improve cycling endurance.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 39 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:255251 HCAPLUS
DN 134:274487
TI Dense SOI **flash memory** array structure with its fabrication and programming
IN Noble, Wendell P.
PA Micron Technology, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6215145	B1	20010410	US 1998-55347	19980406
	US 6255171	B1	20010703	US 1999-414426	19991007
PRAI	US 1998-55347	A3	19980406		

AB A nonvolatile **flash memory** array having Si device islands isolated from the substrate by an insulator. Each island comprises a split-gate transistor with a control **gate** and **floating gate** formed in the upper portion of the island, and **source**, **drain** and channel regions formed in a lower portion of the island. High array d. is achieved by forming **source** and **drain** interconnects in the space between the islands. Also disclosed are processes for forming and programming such arrays.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 40 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:222045 HCAPLUS
DN 134:230746
TI **Flash memory** cells having modulation doped heterojunction structure
IN Fastow, Richard
PA Advanced Micro Devices, Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6207978	B1	20010327	US 2000-516472	20000301

AB The **flash memory** device includes a modulation-doped

heterostructure formed in a semiconductor substrate, a **layer** of tunnel **oxide**, a **floating gate**, a **layer** of **dielec.**, a control gate and **source** and **drain** regions formed in the substrate.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 41 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:221947 HCAPLUS
DN 134:230714
TI Method for shrinking array dimensions of split gate **flash memory** device using multilayer etching to define cell and **source** line
IN Hsieh, Chia-Ta; Lin, Yai-Fen; Sung, Hung-Cheng; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6207503	B1	20010327	US 1998-133970	19980814
	US 2001015455	A1	20010823	US 2001-755281	20010108
PRAI	US 1998-133970	A3	19980814		

AB A method of forming split gate electrode MOSFET devices comprises the following steps. Form a **tunnel oxide layer** over a semiconductor substrate. Form a **floating gate** electrode **layer** over the **tunnel oxide layer**. Form a masking cap over the **floating gate** electrode layer. Pattern a gate electrode **stack** formed by the **tunnel oxide layer** and the **floating gate** electrode layer in the pattern of the masking cap. Form intermetal **dielec.** and control gate **layers** over the substrate covering the **stack** and the **source** regions and the **drain** regions. Pattern the intermetal **dielec.** and control gate **layers** into adjacent mirror image split gate electrode pairs. Pattern a **source** line slot in the center of the gate electrode **stack** down to the substrate. Form **source** regions through the **source** line slot. Form **drain** regions self-aligned with the split gate electrodes and the gate electrode **stack**.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 42 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:178401 HCAPLUS
DN 134:201636
TI Method of fabricating a split-gate **flash memory**
IN Huang, Chih-mu; Tsai, Jung-yu; Renn, Shing-hwa; Lin, Shu-huei
PA Winbond Electronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6200859	B1	20010313	US 1999-454419	19991203
	TW 432512	B	20010501	TW 1999-88119924	19991116
PRAI	TW 1999-88119924	A	19991116		

AB A split-gate **flash memory** is formed by a method described in the following steps. A tunneling **oxide layer**, a 1st conductive layer, and a hard mask layer are formed on a substrate in sequence. A **drain** opening and a **floating gate** opening are formed on the hard mask layer by defining the hard mask layer to expose the 1st conductive layer. A 1st polyoxide layer and a 2nd polyoxide layer are formed on the 1st conductive layer exposed by the **drain** opening and the **floating gate** opening, resp. The 1st polyoxide layer and the 1st conductive layer beneath the 1st polyoxide layer are removed to expose the substrate in the **drain** opening. A **drain** region is formed in the substrate in the **drain** opening. The hard mask layer is removed, and the 1st conductive layer is etched into a **floating gate** using the 2nd polyoxide layer as a mask. A split-gate **oxide layer** and a 2nd conductive layer are formed on the resulting structure in sequence. A control gate is formed by defining the 2nd conductive layer, and a **source** region beside the **floating gate** is formed in the substrate.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 43 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:179813 HCAPLUS
DN 134:201637
TI Method of fabricating self-aligned stacked gate **flash memory** cell
IN Chen, Bin-shing
PA Winbond Electronics Corp., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6200856	B1	20010313	US 1998-123852	19980728
	TW 406420	B	20000921	TW 1999-88102844	19990225
PRAI	US 1998-79290P	P	19980325		
	US 1998-123852	A	19980728		

AB A technique for forming an integrated circuit device having a self-aligned gate **layer** and an overlying **stacked** gate. The method includes a variety of steps such as providing a substrate, which is commonly a Si wafer. Field isolation regions including a 1st isolation region and a 2nd isolation region are defined in the semiconductor substrate. A recessed region is defined between the 1st and 2nd isolation regions. The isolation regions are made using a local oxidn. of Si process, which is commonly called LOCOS, but can be others. A thickness of such as polysilicon is deposited overlying or on the 1st isolation region, the 2nd isolation region, and the active region. A step of selectively removing portions of the thickness of material overlying portions of the 1st isolation region and the 2nd isolation region is performed, where the removing step forms a substantially planar material region in the recessed region. A **stacked** control gate **layer** is formed overlying the thickness of material.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 44 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:131171 HCAPLUS
DN 134:156511
TI Method to fabricate a **flash memory** cell with a planar

stacked gate
IN Lin, Chrong Jung; Chen, Jong; Su, Hung-der; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6190969	B1	20010220	US 1999-257722	19990225
	US 2001012661	A1	20010809	US 2001-760309	20010116
PRAI	US 1999-257722	A3	19990225		

AB A new method of fabricating a **stacked** gate Flash EEPROM device having an improved **stacked** gate topol. is described. Isolation regions are formed on and in a semiconductor substrate. A **tunneling oxide layer** is provided on the surface of the semiconductor substrate. A 1st polysilicon layer is deposited overlying the **tunneling oxide layer** . The 1st polysilicon layer is polished away until the top surface of the polysilicon is flat and parallel to the top surface of the semiconductor substrate. The 1st polysilicon layer is etched away to form the **floating gate**. The **source** and **drain** regions are formed within the semiconductor substrate. An interpoly **dielec. layer** is deposited overlying the 1st polysilicon layer. A 2nd polysilicon layer is deposited overlying the interpoly **dielec. layer**. The 2nd polysilicon **layer** and the interpoly **dielec. layer** are etched away to form a control **gate** overlying the **floating gate**. An **insulating layer** is deposited overlying the **oxide layer** and the control gate. Contact openings are formed through the **insulating layer** to the underlying control gate and to the underlying **source** and **drain** regions. The contact openings are filled with a conducting layer to complete the fabrication of the Flash EEPROM device.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 45 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:25727 HCAPLUS
DN 134:94245
TI Method for forming a **stacked** gate of a **flash** **memory** cell
IN Ding, Yen-lin; Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6171909	B1	20010109	US 1999-293434	19990416
	TW 407381	B	20001001	TW 1999-88103048	19990301
PRAI	TW 1999-88103048	A	19990301		

AB A method for forming a **stacked** gate of a **flash** **memory** cell is described. A 1st **dielec. layer** , a conductive **layer** and a Si nitride layer are sequentially formed over a substrate. A photoresist pattern is formed over the Si nitride layer. The Si nitride **layer**, conductive **layer** , 1st **dielec. layer** and substrate are etched by using

the photoresist pattern as an etching mask until forming a plurality of **trenches** in the substrate. An **insulating layer** is formed over the substrate, in which the **insulating layer** has a surface level between a top surface of the conductive layer and a bottom surface of the conductive layer. A conductive spacer is formed on the sidewalls of the conductive layer and Si nitride layer, in which the conductive spacer and conductive layer serve as a 1st gate conductive layer. The Si nitride layer is removed. A 2nd **dielec** . **layer** and a 2nd gate conductive layer are formed over the substrate. The 2nd gate conductive **layer**, 2nd **dielec.** **layer** and 1st gate conductive layer are patterned to form a control gate, a patterned **dielec.** **layer** and a **floating gate**, resp.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 46 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:336867 HCAPLUS
DN 134:319761
TI Nonvolatile semiconductor memory device
IN Iijima, Kenji
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001127260	A2	20010511	JP 1999-303630	19991026

AB The invention relates to a nonvolatile semiconductor memory device, i.e., a ferroelec. EEPROM or **flash memory**, suited for use in portable information terminal devices, wherein the ferroelec. layer consists of (Pb,Zr,Ti)O3.

L59 ANSWER 47 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:525822 HCAPLUS
DN 135:250264
TI Stack gate PZT/**Al2O3** one transistor ferroelectric memory
AU Chin, Albert; Yang, M. Y.; Sun, C. L.; Chen, S. Y.
CS Department of Electronics Engineering, National Chiao Tung University, Hsinchu, 300, Taiwan
SO IEEE Electron Device Letters (2001), 22(7), 336-338
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A single transistor ferroelec. memory using stack gate PZT/**Al2O3** structure is developed. For the same .apprx.40 .ANG. dielec. thickness, the PZT/**Al2O3**/Si gate dielec. has much better C-V characteristics and larger threshold voltage shift than those of PZT/SiO2/Si. Besides, the ferroelec. MOSFET also shows a large output current difference between programmed on state and erased off state. The <100 ns erase time is much faster than that of **Flash** **memory** where the switching time is limited by erase time.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 48 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:874230 HCAPLUS
DN 134:50046

TI Design and fabrication of a semiconductor **flash memory** device
IN Chang, Kuang-yeh
PA United Microelectronics Corp., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6160287	A	20001212	US 1998-207112	19981208

AB A design and fabrication method are presented for a **flash memory** device. A tunnel **oxide layer** covers a part of a substrate. The tunnel **oxide layer** is covered by a **floating gate**. A 1st inter-poly **dielec**. **layer** is on the **floating gate** . A controlling gate is on the 1st inter-poly **dielec**. **layer** and extending in a strip shape along a 1st direction. A 2nd inter-poly **dielec**. **layer** covers a 1st side wall of the **floating gate**, the 1st inter-poly **dielec**. **layer**, and the controlling gate. A polysilicon spacer is formed covering the 2nd inter-**dielec**. **layer**. A **drain** region is next to a 2nd side wall of the **floating gate** the 1st interpoly **dielec**. **layer**. and the controlling gate in the substrate. A **source** region is next to the spacer in the substrate. A select gate covering the controlling gate, the tunnel **oxide layer**. and the spacer extends along a 2nd direction perpendicular to the 1st direction.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 49 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:874167 HCAPLUS
DN 134:35955
TI Method of fabricating **flash memory** with a self-aligned **source** and elimination of alignment margin between word and **source** lines
IN Hong, Gary; Ko, Joe
PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6159803	A	20001212	US 1998-186404	19981104
PRAI TW 1997-86118768	A	19971212		

AB A method of fabricating a **flash memory**. A semiconductor substrate having a field **oxide layer** which comprises a plurality of parallel oxide lines, a plurality of parallel word lines perpendicular to the parallel **oxide** lines, a **dielec**. **layer** having a same structure as and under the word lines, a plurality of **floating gates** sepd. by the field **oxide layer** from each other under the **dielec**. **layer**, and a plurality of regions encompassed by the field oxide laver and the word lines is provided. A 1st step of ion implantation to the substrate was performed by using the word lines as masks, so that a plurality of **source** regions and a plurality of **drain** regions are formed beside the word lines. Whereas each of

the **source** regions and each of the **drain** regions are formed in the regions encompassed by the field **oxide layer** and the word lines. A photoresist layer is formed to cover the **drain** regions. A 2nd step of ion implantation to the substrate was performed by using the photoresist layer and the parallel word lines as masks. The photoresist layer is removed.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 50 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:830370 HCAPLUS
DN 133:368487
TI Method to increase the coupling ratio of word line to **floating gate** by lateral coupling in **stacked**-gate **flash memory**
IN Hsieh, Chia-Ta; Kuo, Di-Son; Lin, Yai-Fen; Lin, Chrong Jung; Chen, Jong; Su, Hung-Der
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6153494	A	20001128	US 1999-310257	19990512

AB A method is provided for forming a **stacked**-gate **flash memory** cell having a shallow **trench** isolation with a high-step of oxide and high lateral coupling. This is accomplished by 1st depositing an unconventionally high or thick layer of nitride and then forming a shallow **trench** isolation (STI) through the nitride layer into the substrate, filling the STI with isolation oxide, removing the nitride thus leaving behind a deep opening about the filled STI, filling conformally the opening with a 1st polysilicon layer to form a **floating gate**, forming interpoly **oxide layer** over the **floating gate**, and then forming a 2nd polysilicon layer to form the control gate and finally forming the self-aligned source of the **stacked**-gate **flash memory** cell of the invention. A **stacked**-gate **flash memory** cell is also provided having a shallow **trench** isolation with a high-step of oxide and high lateral coupling.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 51 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:830356 HCAPLUS
DN 133:368478
TI **Floating gate** engineering to improve **tunnel** oxide reliability for **flash memory** devices
IN He, Yue-Song; Chang, Kent K.; Huang, Jiahua
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6153470	A	20001128	US 1999-374059	19990812

AB A method of forming **floating gate** to improve

tunnel oxide reliability for **flash memory** devices. A substrate having a **source, drain,** and channel regions is provided. A **tunnel oxide layer** is formed over the substrate. A **floating gate** is formed over the **tunnel** oxide and the channel region, the **floating gate** being multi-layered and having a 2nd layer sandwiched between a 1st layer and a 3rd layer. The 1st layer of the **floating gate** overlying the **tunnel oxide layer** includes an undoped or lightly doped material. The 2nd layer is highly-doped. The 3rd layer is in direct contact with a **dielec. layer,** e.g., an **oxide**-nitride-oxide **stack,** and is made of an undoped or lightly doped material. A dielec. material is formed over the **floating gate** and a control gate is formed over the dielec. material.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 52 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:785888 HCAPLUS
DN 133:328511
TI Method for forming **flash memory** of ETOX cell programmed by band-to-band **tunneling** induced substrate hot electron and read by gate induced **drain** leakage current
IN Chi, Min-hwa
PA Taiwan Semiconductor Manufacturing Corp., Taiwan
SO U.S., 12 pp., Cont.-in-part of U.S. Ser. No. 378,197.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6143607	A	20001107	US 1999-411133	19991001
	US 6084262	A	20000704	US 1999-378197	19990819
	TW 457597	B	20011001	TW 2000-89113214	20000704
PRAI	US 1999-378197	A2	19990819		
	US 1999-411133	A	19991001		

AB A method of forming an ETOX-cell in a semiconductor substrate is disclosed. The method begins with forming a p-well in the substrate. Then, a **drain** region and a **source** region is formed in the p-well. The **drain** region is of a 1st dopant type and the **source** region is of a 2nd dopant type (i.e. same as the dopant type of the p-well). A **floating-gate** and **tunnel** oxide **stack** is formed above the p-well, the **floating gate** formed between the **drain** region and the **source** region and only after the **drain** region and the **source** region have been formed. The **floating gate** is doped with the same dopant type as the p-well. Finally, a control gate is formed above the **floating-gate,** the **floating-gate** and the control gate sepd. by a **dielec. layer.** The new ETOX cells can be organized into a NOR array, but with no need of **source** line connections. Each cell is programmed by band-to-band induced substrate hot-electron (BBISHE) at the **source,** and read by GIDL at the **drain** side.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 53 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:736215 HCAPLUS
DN 133:289946

TI Method for forming mirror image split gate **flash memory** devices by forming a central **source** line slot
IN Hsieh, Chia-Ta; Lin, Chrong Jung; Chen, Shui-Hung; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6133097	A	20001017	US 1998-133969	19980814
US 6326662	B1	20011204	US 2000-633643	20000807

PRAI US 1998-133969 A3 19980814
AB A method of forming split gate electrode MOSFET devices comprises the following steps. Form a **tunnel oxide layer** over a semiconductor substrate. Form a **floating gate** electrode **layer** over the **tunnel oxide layer**. Form a masking cap over the **floating gate** electrode layer. Pattern gate electrode **stacks** formed by the **tunnel oxide layer** and the **floating gate** electrode layer in the pattern of the masking cap. Pattern **source** line slots in the center of the gate electrode **stacks** down to the substrate. Form **source** regions at the base of the **source** lines slots. Form intermetal **dielec**. and control gate **layers** over the substrate covering the **stacks**. Pattern the intermetal **dielec**. and control gate **layers** into adjacent mirror image split gate electrode pairs. Form self-aligned **drain** regions.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 54 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:738863 HCAPLUS
DN 133:289979
TI Process for simultaneously fabricating a stack gate **flash memory** cell and salicided peripheral devices
IN Su, Hung-der; Chen, Jong; Lin, Chrong-jung; Kuo, Di-son
PA Taiwan
SO U.S., 22 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6133096	A	20001017	US 1998-208917	19981210

AB A process for integrating the fabrication of a **flash memory** cell, on a 1st region of a semiconductor substrate, with the fabrication of salicided peripheral devices, on a 2nd region of the semiconductor substrate, was developed. The **flash memory** cell features self-aligned contact structures, located between stacked gate structures, contacting underlying **source/drain** regions. The stack gate structures are comprised of a polycide control gate shape, on a **dielec. layer**, overlying a polysilicon **floating gate** shape. The performance of the peripheral devices are increased via use of metal silicide layers, located on the top surface of a polysilicon gate structure, as well as on the adjacent heavily doped **source/drain** regions.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 55 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:716126 HCAPLUS
DN 133:275232
TI Clean process for manufacturing split-gate **flash memory** device with a **floating gate** electrode with a sharp peak
IN Hsieh, Chia-Ta; Sung, Hung-Cheng; Lin, Yai-Fen; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6130132	A	20001010	US 1998-55439	19980406
	US 6441429	B1	20020827	US 2000-621378	20000721
PRAI	US 1998-55439	A3	19980406		

AB The following steps were used to form a split gate electrode MOSFET device. First form a **tunnel oxide layer** over a semiconductor substrate. Over the **tunnel oxide layer**, form a doped 1st polysilicon layer with a top surface upon which a native oxide forms. Then as an option, remove the native **oxide layer**. On the top surface of the 1st polysilicon layer, form a Si nitride layer and etch the Si nitride layer to form it into a cell-defining layer. Form a polysilicon oxide dielec. cap over the top surface of the 1st polysilicon layer. Aside from the polysilicon oxide cap, etch the 1st polysilicon **layer** and the **tunnel oxide layer** to form a **floating gate** electrode **stack** in the pattern of the masking cap forming a sharp peak on the periphery of the **floating gate** electrode. Form spacers on the sidewalls of the gate electrode **stack**. Then form blanket inter-polysilicon dielec. and blanket control gate layers covering exposed portions of the substrate and covering the **stack**. Pattern the inter-polysilicon **dielec**. and control gate **layers** into a split gate electrode pair. Form a **source** region self-aligned with the **floating gate** electrode **stack**; perform a W silicide anneal; and form a **drain** region self-aligned with the control gate electrodes.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 56 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:699146 HCAPLUS
DN 133:260387
TI Method for forming vertical channel **flash memory** cell using p/n junction isolation
IN Lin, Chrong-jung; Chen, Jong; Chen, Shui-hung; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6127226	A	20001003	US 1997-995998	19971222

AB This is a method of forming a vertical memory device on a semiconductor substrate. Start by forming an initial mask with a first array of parallel strips, with a first orientation, on the surface of a silicon **oxide layer** on a substrate. Then form another mask with transverse strips to form gate trench openings between the first array of strips and the transverse strips. Next, etch **floating gate** trenches in the substrate through the gate trench openings. Dope the walls of the trenches with a threshold implant and remove exposed portions of the mask. Form **source/drain** regions in the substrate self-aligned with the **floating gate** electrode. Strip the remainder of the masks. Form a tunnel **oxide layer** on the trench surfaces and a **floating gate** electrode in the trench on the tunnel **oxide layer**. Above the **source/drain** regions, form **source drain** conductor lines in the substrate in a parallel array. Form an ONO **dielec. layer** and a control gate electrode over the top surface of the **floating gate** electrode and an array of P/N isolation regions in the silicon semiconductor substrate.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 57 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:636184 HCAPLUS
DN 133:216527
TI Fabrication of high capacitive-coupling ratio and high-speed **flash memories** with a textured tunnel oxide
IN Wu, Shye-lin
PA Texas Instruments-Acer Incorporated, Taiwan
SO U.S., 9 pp., Cont.-in-part of U.S. 5,970,342.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6117731	A	20000912	US 1999-270908	19990315
	US 5970342	A	19991019	US 1998-36027	19980306
PRAI	US 1998-36027	A2	19980306		

AB The method includes patterning a gate structure. Then, a polyoxide layer is formed on side walls of the gate structure. Then, silicon nitride side wall spacers are formed on the side walls of the gate structure. Then, **source/drain** structure of the device is fabricated. Next, the side wall spacers are removed to expose a portion of the **source** and **drain**. Then, an undoped amorphous silicon layer is formed on the surface of the gate structure, the **oxide layer** and the exposed **source** and **drain**. A dry oxidn. process is used to convert the amorphous silicon **layer** into textured tunnel **oxide** at the interface of the substrate and the oxide. The oxide is then removed, and a further **oxide layer** is re-deposited on the gate and substrate. Polysilicon side wall spacers are then formed. A further polysilicon layer is subsequently deposited over the gate. Then, the polysilicon layer is patterned to define the **floating gate**. A dielec. is formed at the top of the **floating gate**. A conductive layer is formed on the **dielec. layer** as the control gate.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 58 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:529226 HCAPLUS
DN 133:113678

TI Field effect transistor having a **floating gate** for split-gate **flash memory** cell and its fabrication
IN Hsu, Louis L.; Mandelman, Jack A.; Hu, Chih-Chun
PA International Business Machines Corporation, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6097056	A	20000801	US 1998-67571	19980428
	US 6245613	B1	20010612	US 2000-556698	20000424
PRAI	US 1998-67571	A3	19980428		

AB A field effect transistor which comprises a semiconductor substrate having a **source** region and a **drain** region sepd. by a channel region; a conductive **floating gate** formed over a 1st portion of the channel region adjacent to the doped **source** region and recessed into the semiconductor substrate; and being sepd. from the 1st portion of the channel region by a 1st **insulation layer**; and a conductive control gate formed substantially over but elec. isolated from the **floating gate** and formed over the entire channel region; along with a method for fabricating such is provided.
RE.CNT 45 THERE ARE 45 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 59 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:508212 HCAPLUS
DN 133:98167
TI Fabrication of split-gate **flash memory** with minimum over-erase problem and improved coupling efficiency
IN Yang, Yu-hao
PA Windbond Electronics Corp., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6093945	A	20000725	US 1998-113032	19980709
	TW 407380	B	20001001	TW 1998-87115926	19980924
	US 6329248	B1	20011211	US 2000-528515	20000320
PRAI	US 1998-113032	A	19980709		

AB A split-gate semiconductor **flash memory** contains an outwardly-diverging control gate **stacked** on but sepd. from a pair of opposing **floating gates** via an inter-poly **dielec. layer**. The split-gate **flash memory** is formed by (a) forming a 1st **dielec. layer** having a **trench** region on a substrate; (b) forming a **tunnel oxide layer** (ETOX) in the **trench** region; (c) forming a 1st polysilicon **layer** covering the 1st **dielec. layer** and the **tunnel oxide layer**; (d) applying an anisotropic etching technique on the 1st polysilicon layer to form a pair of opposing polysilicon sidewall spacers on the sidewalls which will eventually become **floating gates**;. (e) depositing an inter-poly **dielec. layer** on the polysilicon sidewall spacers and the **tunnel oxide layer**; (f) filling the channel area between the pair of polysilicon sidewall spacers with a 2nd

polysilicon layer; (g) planarizing the 2nd polysilicon layer so that relative to the 1st **dielec. layer** to form a control gate; (h) removing the 1st **dielec. layer**, capping the control **gate** and the **floating gate** with a final **oxide layer**, and forming **source** and **drain** regions in the substrate using ion implantation. The split-gate **flash memory** eliminates the over-erase problem experienced with the self-aligned ETOX **flash memory** cells, while allowing its cell dimension to maintain at least the same using the conventional photolithog. technique.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 60 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:508175 HCAPLUS
DN 133:98151
TI Method of manufacture of vertical **stacked** gate **flash memory** device
IN Lin, Chrong-jung; Chen, Shui-hung; Liang, Mong-song
PA Taiwan Semiconductor Manufacturing Co., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6093606	A	20000725	US 1998-35049	19980305

AB A method of forming a vertical transistor memory device comprises the following process steps. Before forming the **trenches**, FOX regions are formed between the rows. Then form a set of **trenches** with sidewalls and a bottom in a semiconductor substrate with threshold implant regions the sidewalls. Form doped **drain** regions near the surface of the substrate and doped **source** regions in the base of the device below the **trenches** with oppositely doped channel regions there between. Form a **tunnel oxide layer** over the substrate including the **trenches**. Form a blanket thin **floating gate** layer of doped polysilicon over the **tunnel oxide layer** extending above the **trenches**. Etch the **floating gate** layer leaving upright **floating gate** strips of the **floating gate** layer along the sidewalls of the **trenches**. Form an interelectrode **dielec. layer** composed of ONO over the **floating gate** layer and over the **tunnel oxide layer**. Form a blanket thin control gate layer of doped polysilicon over the interelectrode **dielec. layer**. Pattern the control gate layer into control gate electrodes. Form spacers adjacent to the sidewalls of the control gate electrode.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 61 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:467845 HCAPLUS
DN 133:67351
TI Manufacture of vertical split gate **flash memory** device
IN Jung, Lin Chrong; Chen, Shui-Hung; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent

LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6087222	A	20000711	US 1998-35058	19980305
	US 6391719	B1	20020521	US 2000-575963	20000523
	US 2002151136	A1	20021017	US 2002-117889	20020408
PRAI	US 1998-35058	A3	19980305		

AB A method of forming a vertical transistor memory device includes the following steps. Before forming the trenches, field oxide (FOX) regions are formed between the rows. Form a set of trenches with sidewalls and a bottom in a semiconductor substrate with threshold implant regions the sidewalls. Form doped **drain** regions near the surface of the substrate and doped **source** regions in the base of the device below the trenches with oppositely doped channel regions therebetween. Form a tunnel **oxide layer** over the substrate including the trenches. Form a blanket thick **floating gate** layer of doped polysilicon over the tunnel **oxide layer** filling the trenches and extending above the trenches. Etch the **floating gate** layer down below the top of the trenches. Form an interelectrode **dielec. layer** composed of ONO over the **floating gate** layer and over the tunnel **oxide layer**. Form a blanket thick control gate layer of doped polysilicon over the interelectrode **dielec. layer** . Pattern the control gate layer into control gate electrodes. Form spacers adjacent to the sidewalls of the control gate electrode.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 62 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:304343 HCAPLUS
DN 132:302036
TI Stacked gate structure for **flash memory** application and fabrication
IN Huang, Richard J.
PA Advanced Micro Devices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6060741	A	20000509	US 1998-154072	19980916

AB To form a low resistance gate for use in a flash EPROM or EEPROM, a B doped amorphous Si layer is formed on an oxide layer and a layer of W nitride formed thereon. A layer of W silicide is then formed on the W nitride layer acts as a barrier preventing out diffusion of a contaminating dopant, e.g., B, and exhibits good adhesion to the amorphous Si layer. The W silicide layer, in turn, exhibits good adhesion to the W nitride layer thereby preventing lifting of the silicide layer and dopant penetration.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 63 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:252980 HCAPLUS
DN 132:259377
TI Fabrication of a large planar area ONO interpoly dielectric in a **flash memory** device
IN Chan, Lap; Cha, Cher Liang

PA Chartered Semiconductor Manufacturing, Ltd., Singapore; National University of Singapore
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6051467	A	20000418	US 1998-53855	19980402
	SG 71836	A1	20000418	SG 1998-3588	19980909
PRAI	US 1998-53855	A	19980402		

AB A new method of fabricating a stacked gate flash EEPROM device having an improved interpoly **oxide layer** is described. A gate **oxide layer** is provided on the surface of a semiconductor substrate. A 1st polysilicon layer is deposited overlying the gate **oxide layer**. The 1st polysilicon layer is etched away where it is not covered by a mask to form a **floating gate**. **Source** and **drain** regions assocd. with the **floating gate** are formed within the substrate. An **oxide layer** is deposited overlying the **floating gate** and the substrate. The **oxide layer** is polished away until the top of the **oxide layer** is even with the top of the **floating gate**. A 2nd polysilicon layer is deposited overlying the **oxide layer** and the 1st polysilicon layer of the **floating gate**; the 2nd polysilicon layer has a smooth surface. An interpoly **dielec. layer** is deposited overlying the 2nd polysilicon layer. A 3rd polysilicon layer is deposited overlying the interpoly **dielec. layer**. The 3rd polysilicon **layer** and the interpoly **dielec. layer** are etched away where they are not covered by a mask to form a control **gate** overlying the **floating gate**. An **insulating layer** is deposited overlying the **oxide layer** and the control gate. Contact openings are formed through the **insulating layer** to the underlying control gate and to the underlying **source** and **drain** regions. The contact openings are filled with a conducting layer to complete the fabrication of the flash EEPROM device.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 64 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:238023 HCAPLUS
DN 132:245023
TI **Flash memory** device having high permittivity stacked dielectric and fabrication thereof
IN Gardner, Mark I.; Gilmer, Mark C.; Spikes, Thomas E., Jr.
PA Advanced Micro Devices, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6048766	A	20000411	US 1998-172410	19981014

AB A memory device having a high performance stacked dielec. sandwiched between two polysilicon plates and method of fabrication thereof is provided. A memory device, in accordance with an embodiment, includes two polysilicon plates and a high permittivity dielec. stack disposed between the two polysilicon plates. The high permittivity dielec. stack includes

a relatively high permittivity layer and two relatively low permittivity buffer layers. Each buffer layer is disposed between the relatively high permittivity layer and a resp. one of the two polysilicon plates. The high permittivity layer may, for example, be a barium strontium titanate and the buffer layers may each include a layer of silicon nitride adjacent the resp. polysilicon plate and a layer of titanium dioxide between the silicon nitride and the barium strontium titanate. The new high performance dielec. layer can, e.g., increase the speed and reliability of the memory device as compared to conventional memory devices.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 65 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:167123 HCAPLUS
DN 132:201894
TI **Stack** gate **flash memory** cell featuring symmetric self-aligned contact structures
IN Su, Hung-Der; Lin, Chrong-Jung; Chen, Jong; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6037223	A	20000314	US 1998-177342	19981023

AB A process for fabricating a **flash memory** cell featuring self-aligned contact structures overlying and contacting self-aligned **source**, and self-aligned **drain** regions located between **stack** gate structures has been developed. The **stack** gate structures located on an underlying **silicon dioxide tunnel oxide layer** comprise: a capping **insulator** shape; a polysilicon control gate shape; an inter-polysilicon dielec. shape; and a polysilicon **floating gate** shape. The use of self-aligned contact structures and self-aligned **source** regions allows increased cell densities to be achieved.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 66 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:10680 HCAPLUS
DN 132:72260
TI Metal oxide **stack** for **flash memory** application
IN Huang, Richard J.; Shen, Lewis
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6011289	A	20000104	US 1998-154073	19980916

AB To alleviate lifting problems and to reduce the height of the **stack**, a W **layer** is formed on an interpoly **dielec. layer**, such as an ONO layer, which separates the conductive control gate from a polysilicon **floating gate** that is in turn formed on a **tunnel oxide layer**

. The W layer is protected by the provision of a W silicide cap which is formed over the W layer and which therefore prevents oxidn. of the metal. The 2 W-based layers replace the 2nd polysilicon layer which is normally used to form the **floating gate**.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 67 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:10679 HCAPLUS
DN 132:72259
TI **Flash memory** cell with vertical channels and **source/drain** bus lines
IN Lin, Chrong-Jung; Chen, Shui Hung; Chen, Jong; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6011288	A	20000104	US 1997-995999	19971222
	US 6066874	A	20000523	US 1999-407108	19990927
PRAI	US 1997-995999		19971222		

AB A vertical memory device on a Si substrate comprises a **floating gate** trench in the substrate. The walls of the **floating gate** trench are doped with a threshold implant through the trench surfaces. There is a tunnel **oxide layer** on the trench surfaces. There is a **floating gate** electrode in the trench on the outer surfaces of the tunnel **oxide layer**. There are **source/drain** regions in the substrate self-aligned with the **floating gate** electrode. A **source** line and a **drain** line are formed above the **source** region and the **drain** region, resp. An interelectrode **dielec. layer** overlies the **floating gate** electrode, the **source** line, and the **drain** line, and there is a control gate electrode over the interelectrode **dielec. layer** over the **floating gate** electrode.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 68 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:650537 HCAPLUS
DN 137:162272
TI The **flash memory** process with MIM structure
IN Wu, Shie-Lin
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 25 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 404058	B	20000901	TW 1999-88105884	19990413

AB This invention comprises forming the gate pattern; then, form the oxide on the sidewall of gate structure; next, form a silicon nitride spacer on the sidewall of the gate structure; next, form the source and drain. Next, remove the spacer and form an undoped amorphous silicon layer on the surface of the gate structure, oxide and the exposed source and drain.

Transform the amorphous silicon layer into the tunnel oxide with a rough interface in the semiconductor substrate. A poly-silicon layer is subsequently deposited on the substrate; next, perform a chem. mech. polishing process to polish the above-mentioned poly-silicon to at least expose the gate. Next, form an elec. conductive structure on the above-mentioned structure, a silicon nitride deposited by using JVD technique is deposited on the above-mentioned elec. conductive layer as the barrier layer, a dielecs. is next deposited on the above-mentioned JVD silicon nitride layer as high elec. const. film layer. An elec. conductive layer was used as the control gate and is formed on the above-mentioned high elec. const. film layer.

L59 ANSWER 69 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:732000 HCAPLUS
DN 137:225186
TI Method for manufacturing the gates separated **flash memory** with tipped floating gate
IN Shie, Jia-Da; Lin, Ya-Fen; Sung, Hung-Jeng; Ye, Juang-Ge; Guo, Di-Sheng
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 21 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 401593	B	20000811	TW 1999-88103012	19990226

AB A tipped floating age sepd. **flash memory** device is fabricated by first forming an oxide pad layer and a nitride layer on the semiconductor wafer. Defining the location of the floating gate. Removing the oxide layer between defined gate region; and forming a dielec. layer and filling with polysilicon layer, followed by planarization. Oxide region is produced by thermal oxidn., the unoxidized region and nitride region and pad oxide are removed. The oxidized polysilicon layer and a 2nd polysilicon layer are form. The control gate is defined in the formation of **flash memory** gate structure. The device is completed by ion implantation.

L59 ANSWER 70 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:691562 HCAPLUS
DN 137:193797
TI Method to improve the coupling ratio of wordline of **stacked** gate **flash memory** element to **floating gate**
IN Shie, Jia-Da; Guo, Di-Shen; Lin, Ya-Fen; Lin, Chung-Rung; Chen, Jung
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 29 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 388131	B	20000421	TW 1998-87118326	19981104

AB The present invention provides a method to improve the coupling ratio of the wordline of a **stacked** gate **flash memory** element to a **floating gate** while reducing the voltage of the wordline. The invented method at least comprises the following steps: sequentially forming a 1st **oxide layer**, a 1st nitride layer on a semiconductor wafer; defining a **trench** isolation region; sequentially forming a thin **oxide layer** clad on the **trench** isolation region; filling up

the **trench** isolation region with a 2nd **oxide layer**; using the 1st nitride layer as the stop layer to carry out a planarization process; etching the 1st nitride layer, and then etching the 1st **oxide layer** using the 1st **oxide layer** as the stop layer to expose the surface of the wafer; forming a gate **oxide layer** of good quality on the wafer by a thermal oxidn. process; forming a 1st polysilicon layer with a suitable thickness on the gate **oxide layer** and the 2nd **oxide layer**; etching the 1st polysilicon **layer** on the 2nd **oxide layer** thereby isolating the 1st polysilicon layer from the **trench** isolation region; forming an ONO inter-polysilicon **oxide layer** on the 1st polysilicon layer; forming a 2nd polysilicon layer; covering the 2nd polysilicon layer with a photoresist pattern exposing a predetd. wordline to carry out a **stacked** gate etching; and carrying out a common **source** etching and applying a **source/drain** implantation and an annealing treatment to form a **stacked** gate **flash memory**.

L59 ANSWER 71 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:550134 HCAPLUS
DN 137:86988
TI Vertical split gate **flash memory** structure and production method therefor
IN Lin, Chung-Rung; Chen, Suei-Hung; Guo, Di-Sheng
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 25 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
TW 386312	B	20000401	TW 1998-87107933	19980522

AB The present invention provides a vertical split gate **flash memory** structure and a prodn. method thereof. The objective of the present invention is to increase the packing d. and solve the problem of misalignment of two layers of polysilicon of the gate electrode. also, the **floating gate** memory structure of the present invention at least comprises: a plurality of trenches where each trench was used to form a control **gate**, a **floating gate** plate and a vertical channel; a mutually connected 1st **source/drain** region on the lower surface of a plurality of trenches, and 2nd **source/drain** region below the upper surface of the wafer, segregated with a plurality of trenches. A plurality of lateral spacers are located in pairs on the two sides of plural trenches protruded on the surface portion of a wafer. The sidewalls of the trenches have a vertical channel. The bottom and the sidewalls of the trenches have a 1st **dielec. layer** therein. The **floating gate** is located on the 1st **dielec. layer** on the bottom of the trench, the 2nd **dielec. layer**, and the control gate (polysilicon) are sequentially formed on the 1st **dielec. layer** of the **floating gate** and the sidewalls of the trenches. The present invention also provides a method of producing such a device.

L59 ANSWER 72 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:828127 HCAPLUS
DN 135:337936
TI **Flash memory** processing method for self-aligned contact **source** and **drain** processing

IN Su, Hung-De; Lin, Chung-Rung; Chen, Jung; Kuo, Di-Sheng
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO Taiwan, 36 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 383468	B	20000301	TW 1998-87114440	19980901

AB A **flash memory** processing for self-aligned contact **source** and **drain** processing includes the following steps: defining active area and forming isolation area on the substrate; forming gate **oxide**; forming substantial Si **layer**; then, removing substantial Si and gate oxide outside the peripheral device area;forming tunneling oxide; forming the 1st Si layer; defining **floating gate**; then, forming gate dielec.; defining overlapped gate structure and removing control gate, gate **dielec** . and 1st Si **layer** on the peripheral device area and proceeding the 1st ion implantation in the dual diffusion **source/ drain** area; defining again the gate structure in the peripheral device area; proceeding ion implantation in the lightly doped **source/drain** area of peripheral device area; proceeding 2nd ion implantation in dual diffusion **source/drain** area; forming sidewall structure; proceeding ion implantation in **source/drain** area in peripheral device area; then, forming silicide layer on the **source/drain** area and substantial Si **layer**; forming inter-**layer dielec**.; defining contact holes; forming again and defining metal layer to form the connections.

L59 ANSWER 73 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:182452 HCAPLUS
DN 136:208983
TI Method for forming tungsten plug for **flash memory** device
IN Ko, Seong Han; Yoon, Jong Won
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI KR 2000044947	A	20000715	KR 1998-61450	19981230

AB A method for forming tungsten plug for **flash memory** device is provided to prevent the surface of an wafer from becoming roughened by chem. soln. in cleaning process, thereby stabilizing following metal wiring forming process. A method for forming tungsten plug for **flash memory** device comprises steps of: forming an interlayer insulation film and a contact hole exposing a portion of a lower conductive layer; forming barrier metal having titanium/titanium nitride stack structure; depositing tungsten; removing the tungsten and titanium nitride film to expose the titanium film; and converting the exposed titanium film into a **titanium oxide** film by oxygen plasma process.

L59 ANSWER 74 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:665944 HCAPLUS
DN 133:260323

TI Nonvolatile semiconductor **flash memory** devices and fabrication thereof
IN Nakagawa, Kenichiro
PA Nec Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000260887	A2	20000922	JP 1999-60546	19990308

AB The title devices have a stripe groove in a space between **source /drain** regions on a semiconductor substrate, a tunnel **insulator film** lined on the sidewalls and the bottom of the groove, and a **floating gate** material buried in the groove on the tunnel **insulator film** so that a channel region is formed around the groove upon functioning by impression of voltage. The formation of the **floating gate** in the groove across the tunnel **insulator film** gives the memory devices prevention of deterioration of the tunnel **insulator film**, prevention of punch-through generation, and increased ON current.

L59 ANSWER 75 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:116498 HCAPLUS
DN 132:159922
TI Manufacture of **flash memory** devices
IN Yuzuriha, Kojiro
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000049243	A2	20000218	JP 1998-214231	19980729

AB Ions are implanted from inclined directions using floating gates and resist patterns as masks to form n+-type regions with offset regions. sidewalls are formed around the floating gates using CVD oxide films which have greater etching rate against **HF, oxide** films are formed by thermal oxidn., the sidewalls are removed with HF, and sidewalls from poly-poly insulator films are formed around the floating gates.

L59 ANSWER 76 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:367140 HCAPLUS
DN 132:355632
TI Nonvolatile memory semiconductor device and manufacture of same
IN Ito, Hiroshi; Sakai, Isami
PA NEC Corporation, Japan
SO Eur. Pat. Appl., 28 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1005081	A2	20000531	EP 1999-123440	19991124
EP 1005081	A3	20010207		

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,

IE, SI, LT, LV, FI, RO

	JP 2000164834	A2	20000616	JP 1998-335835	19981126
	JP 3314807	B2	20020819		
	US 6287907	B1	20010911	US 1999-447869	19991123
	US 2002052073	A1	20020502	US 2001-950870	20010912
PRAI	JP 1998-335835	A	19981126		
	US 1999-447869	A3	19991123		

AB The nonvolatile memory semiconductor device (e.g., flash EEPROM) comprises a **flash memory** area where a memory-transistor and a select-transistor are formed, and a logic area where an adjacent circuit transistor is formed on the same substrate; wherein the memory-transistor is composed of layers of structure consisting of a **floating gate** and a control gate sepd. by a first **insulating film**; and at least a gate electrode of a select-transistor is composed of a single layer of a polysilicon film, which is formed from the same layer as the **floating gate** electrode of the memory-transistor and then doped to have an enhanced dopant concn. by ion implantation performed in the step of forming **source-drain** regions of the transistors.

L59 ANSWER 77 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:691327 HCAPLUS
DN 131:294411
TI Elimination of poly cap for easy poly1 contact for NAND **floating gate** memory
IN Wang, John Jianshi; Fang, Hao; Higashitani, Masaaki
PA Advanced Micro Devices, Inc., USA; Fujitsu Limited
SO PCT Int. Appl., 28 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9954931	A1	19991028	WO 1999-US3043	19990211
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6057193	A	20000502	US 1998-61515	19980416
	EP 1074046	A1	20010207	EP 1999-906961	19990211
	R: DE, FR, GB, NL				
	JP 2002512450	T2	20020423	JP 2000-545192	19990211
	US 6312991	B1	20011106	US 2000-531582	20000321
PRAI	US 1998-61515	A	19980416		
	WO 1999-US3043	W	19990211		

AB A method (200) of forming a NAND type **flash memory** device includes the steps of forming an **oxide layer** (202) over a substrate (102) and forming a 1st conductive **layer** (106) over the **oxide layer**. The 1st conductive layer (106) is etched to form a gate structure (107) in a select gate transistor region (105) and a **floating gate** structure (106a, 106b) in a memory cell region (111). A 1st **insulating layer** (110) is then formed over the memory cell region (111) and a 2nd conductive layer (112, 118) is formed over the 1st **insulating layer** (110). A word line (122) is patterned in the memory cell region (111) to form a control gate region and **source** and **drain** regions (130, 132) are formed in the substrate (102) in a region adjacent the word line (122) and in a region adjacent the gate structure(107). A 2nd **insulating layer** (140) is formed over both the select gate transistor region (105) and the memory cell region (111) and 1st and 2nd contact openings are formed in the 2nd

insulating layer (140) down to the gate structure (107) and the control gate region, wherein a depth (X) through the 2nd **insulating layer** (140) down to the gate structure (107) and down to the control gate region are approx. the same, thereby eliminating a substantial overetch of the gate structure contact opening.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 78 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:818235 HCAPLUS
DN 132:57961
TI Method of forming high density **flash memories** with high capacitive-couping ratio and high speed operation
IN Wu, Shye-Lin
PA Taiwan
SO U.S., 9 pp., Cont.-in-part of U.S. 5,970,342.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6008090	A	19991228	US 1999-261027	19990302
	US 5970342	A	19991019	US 1998-36027	19980306
PRAI	US 1998-36027	A2	19980306		

AB The method of the present invention includes patterning a gate structure. Then, a polyoxide layer is formed on side walls of the gate structure. Then, silicon nitride side wall spacers is formed on the side walls of the gate structure. Then, **source/drain** structure of the device is fabricated. Next, the side wall spacers is removed to expose a portion of the **source** and **drain**. Then, an undoped amorphous silicon layer is formed on the surface of the gate structure, the **oxide layer** and the exposed **source** and **drain**. A dry oxidn. process is used to convert the amorphous silicon **layer** into textured tunnel **oxide** at the interface of the substrate and the oxide. A polysilicon layer is than formed, followed by chem. mech. polishing the layer. A rugged silicon layer is subsequently deposited over the gate and the polished polysilicon. Then, the **floating gate** is defined. A dielec. is formed at the top of the rugged silicon. A conductive layer is formed on the **dielec. layer** as a control gate.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 79 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:779188 HCAPLUS
DN 132:17899
TI Method of forming high density **flash memories** with MIM structure
IN Wu, Shye-Lin
PA Taiwan
SO U.S., 9 pp., Cont.-in-part of U.S. Ser. No. 36,027.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5998264	A	19991207	US 1999-266552	19990311
	US 5970342	A	19991019	US 1998-36027	19980306
PRAI	US 1998-36027	A2	19980306		

AB The method includes patterning a gate structure. Then a polyoxide layer is formed on the sidewalls of the gate structure. Then Si nitride sidewall spacers are formed on the sidewalls of the gate structure. Then the source/drain structure of the device is fabricated. Next, the sidewall spacers are removed to expose portions of the source and drain. Then an undoped amorphous Si layer is formed on the surface of the gate structure, the oxide layer, and the exposed source and drain. A dry oxidn. process is used to convert the amorphous Si layer into textured tunnel oxide at the interface of the substrate and the oxide. A polysilicon layer is then formed, followed by chem. mech. polishing of the layer. A conductive layer is formed on the polysilicon layer. Subsequently, a Si nitride layer deposited by jet vapor deposition (JVD) is formed on the conductive layer. A high-k dielec. layer is next formed on the JVD nitride. A conductive layer to serve as control gate is subsequently formed on the high-k dielec. layer. A patterning technique is used to pattern the layers.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 80 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:761485 HCAPLUS
DN 131:359227
TI Fabrication of **flash memory** cell, especially Zener breakdown based **flash memory**
IN Sheu, Yau-Kae; Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5994185	A	19991130	US 1998-24163	19980217
PRAI	TW 1998-87101623	A	19980207		

AB In the process, a heavily doped region with the opposite polarity of the **drain** region is formed between the channel region and the **drain** region. The heavily doped region is in a bar shape extending towards both the **drain** and the **source** regions along a side of the **floating gate**. Furthermore, the reading operation is performed in reverse by applying a zero voltage to the **drain** region, and a non-zero voltage to the **source** region.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 81 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:718918 HCAPLUS
DN 131:331070
TI Encroachless LOCOS isolation
IN Krivokapic, Zoran
PA Advanced Micro Devices, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5981358	A	19991109	US 1997-965404	19971106
	US 6255711	B1	20010703	US 1999-398916	19990916

PRAI US 1997-965404 A3 19971106
AB This invention provides a fabrication process for an integrated-circuit substrate structure having LOCOS isolation areas formed such that oxidn. encroachment at an active surface region patterned on the substrate is <0.1 .mu.m. The fabrication process includes various steps for forming a (0.75-1.0)-.mu.m layer of **SiO2** over thin layers of **SiO2** (0.01-0.05 .mu.m) and Si nitride (0.05-0.10 .mu.m) over a surface region of the substrate to form a protective **stack**/passivation **layers** over a surface region of the Si substrate. The protected substrate surface region is usable for fabricating a microelectronic circuit device, such as a MOS transistor or a **flash memory** device. Adjacent to the protective stack, a Si nitride spacer region is formed to effectively widen the protected substrate surface region. The Si nitride spacer region limits the encroachment of oxide, commonly called bird's beak growth of oxide, into the active surface region beneath the spacer and protective stack.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 82 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:718911 HCAPLUS
DN 131:316701
TI Sidewall spacer for protecting tunnel oxide during isolation trench formation in self-aligned **flash memory** core
IN Kim, Unsoon; Liu, Yowjuang W.; Sun, Yu; Hui, Angela T.
PA Advanced Micro Devices, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5981341	A	19991109	US 1997-986160	19971205

AB A method for making a self-aligned isolated **flash memory** core without damaging tunnel oxide **layers** between memory element **stacks** and the Si substrate supporting the stacks includes depositing 3 sidewall **layers** on the **stacks**, prior to etching isolation trenches between the stacks, to shield the tunnel oxide during isolation trench etching.
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 83 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:686643 HCAPLUS
DN 131:294307
TI Method of manufacturing a **flash memory** cell having a tunnel oxide with a long narrow top profile to decrease area and increase coupling ratio and lower the operating voltage
IN Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5972752	A	19991026	US 1997-998725	19971229

AB A method for forming a **flash memory** cell structure comprising the steps of providing a semiconductor substrate, and then

sequentially forming a bottom conductive **layer** and a cap **oxide layer** over the substrate. Next, a pattern is defined in the conductive **layer** and the cap **oxide layer**. Subsequently, a thermal oxidn. method was used to form a Si **oxide layer** on the sidewalls of the bottom conductive layer. Then, a gate **oxide layer** is formed between the bottom conductive layers above the substrate. Thereafter, **source/drain** regions are formed in the semiconductor substrate. Then, spacer structures are formed adjacent to the Si **oxide layers**. Using the spacer structures as masks, a portion of the gate **oxide layer** is etched. Then, the spacer structures are removed to expose the gate **oxide layer**. Next, a thermal oxidn. method was used to form a tunneling **oxide layer** in the narrow region between the gate **oxide layer**. The tunneling **oxide layer** has a long narrow top profile. Finally, a **floating gate layer**, a **dielec. layer** and a control gate are sequentially formed to complete the **flash memory** cell structure.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 84 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:670155 HCAPLUS
DN 131:265859
TI Method of forming high capacitive-coupling ratio and high speed **flash memories** with a textured tunnel oxide
IN Wu, Shye-lin
PA Texas Instruments-Acer Incorporated, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5970342	A	19991019	US 1998-36027	19980306
	US 6008090	A	19991228	US 1999-261027	19990302
	US 5998264	A	19991207	US 1999-266552	19990311
	US 6117731	A	20000912	US 1999-270908	19990315
PRAI	US 1998-36027	A2	19980306		

AB The method of the present invention includes patterning a gate structure. Then, a polyoxide layer is formed on side walls of the gate structure. Then, silicon nitride side wall spacers is formed on the side walls of the gate structure. Then, **source/drain** structure of the device is fabricated. Next, the side wall spacers is removed to expose a portion of the **source** and **drain**. Then, an undoped amorphous silicon layer is formed on the surface of the gate structure, the **oxide layer** and the exposed **source** and **drain**. A dry oxidn. process is used to convert the amorphous silicon **layer** into textured tunnel **oxide** at the interface of the substrate and the oxide. Polysilicon side wall spacers are then formed. A further polysilicon layer is subsequently deposited over the gate. Then, the polysilicon layer is patterned to define the **floating gate**. A dielec. is formed at the top of the **floating gate**. A conductive layer is formed on the **dielec. layer** as control gate.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 85 OF 110 HCAPLUS COPYRIGHT 2002 ACS

AN 1999:671063 HCAPLUS
DN 131:280274
TI Method for forming vertical channels in split-gate **flash memory** cell
IN Lin, Chrong-jung; Hsieh, Chia-ta; Chen, Jong; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5970341	A	19991019	US 1997-988772	19971211
	US 6078076	A	20000620	US 1999-317645	19990524
PRAI	US 1997-988772	A3	19971211		

AB A method of forming a vertical memory split gate **flash memory** device, particularly EEPROM device, on a silicon semiconductor substrate is provided by the following steps. Form a **floating gate** trench hole in the silicon semiconductor substrate, the trench hole having trench surfaces. Form a tunnel **oxide layer** on the trench surfaces, the tunnel **oxide layer** having outer surfaces. Form a **floating gate** electrode layer filling the trench hole on the outer surfaces of the tunnel **oxide layer**. Form **source/drain** regions in the substrate self-aligned with the **floating gate** electrode layer. Pattern the **floating gate** electrode layer by removing the gate electrode layer from the **drain** region side of the trench hole. Form a control gate hole therein. Form an interelectrode **dielec. layer** over the top surface of the **floating gate** electrode, and over the tunnel **oxide layer**. Form a control gate electrode over the interelectrode **dielec. layer** over the top surface of the **floating gate** electrode and extending down into the control gate hole in the trench hole.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 86 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:622366 HCAPLUS
DN 131:236801
TI Forming a vertical-channel **flash memory** cell
IN Lin, Chrong Jung; Chen, Shui-hung; Chen, Jong; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5960284	A	19990928	US 1997-985647	19971205
	US 6437397	B1	20020820	US 1999-377539	19990819
PRAI	US 1997-985647	A3	19971205		

AB A vertical memory device on a Si substrate is formed by the following steps. An array of isolation Si oxide structures is formed on the substrate. A **floating-gate** trench is formed in the substrate between the Si oxide structures in the array. The sidewalls of the **floating-gate** trench are doped with a threshold implant through the trench sidewall surfaces. A tunnel **oxide**

layer is formed on the trench sidewall surfaces. A **floating gate** electrode is formed in the trench on the tunnel **oxide layer**. **Source/drain** regions are formed in the substrate self-aligned with the **floating gate** electrode. An interelectrode **dielec. layer** is formed over the top surface of the **floating gate** electrode. A control gate electrode is formed over the interelectrode **dielec. layer**. A **source** line is formed by performing a self-aligned etch followed by a **source** line implant.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 87 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:487154 HCAPLUS
DN 131:109918
TI **Flash memory** cell structure having electrically isolated **stacked** gate
IN Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5932910	A	19990803	US 1997-998772	19971229
PRAI TW 1997-86115423		19971020		

AB This invention provides a **flash memory** cell structure comprising a semiconductor substrate; a **tunneling oxide layer** formed above the substrate and having a long narrow top profile; a gate **oxide layer** formed above the substrate on each side of the **tunneling oxide layer**; a bottom conductive layer formed above the substrate and surrounded the gate **oxide layer**; and a **stacked** gate formed above the **tunneling oxide layer**, the gate **oxide layer** and the bottom conductive layer, wherein there is an **insulating layer** between the **stacked** gate and the bottom conductive layer for elec. isolating the **stacked** gate from the bottom conductive **layer**, and that the **stacked** gate further comprises a **floating gate**, a **dielec. layer** and a control gate.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 88 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:439371 HCAPLUS
DN 131:66552
TI Electronic components with doped metal oxide dielectric materials and a process for making MOS devices with doped metal oxide dielectric materials
IN Lee, Woo-hyeong; Manchanda, Lalita
PA Lucent Technologies Inc., USA
SO U.S., 6 pp., Cont.-in-part of U.S. Ser. No. 871,024.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5923056	A	19990713	US 1998-41434	19980312

	JP 11297867	A2	19991029	JP 1999-65742	19990312
PRAI	US 1996-27612P	P	19961010		
	US 1997-871024	A2	19970606		
	US 1998-41434	A	19980312		

AB A doped, metal oxide dielec. material and electronic components made with this material are disclosed. The metal oxide is a Group III or Group VB metal oxide (e.g. **Al2O3, Y2O3, Ta2O5** or V2O5 and the metal dopant is a Group IV material (Zr, Si, Ti, and Hf)). The metal oxide contains .apprx.0.1 to .apprx.30 wt.% of the dopant. The doped, metal oxide dielec. of the present invention was used in a no. of different electronic components and devices. For example, the doped, metal oxide dielec. was used as the gate dielec. for MOS devices. The doped, metal oxide dielec. is also used as the inter-poly dielec. material for **flash memory** devices.

RE.CNT 24 THERE ARE 24 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 89 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:205275 HCAPLUS
DN 130:216772
TI Process for fabricating SOI compact contactless **flash memory** cell
IN Lin, Ruei-Ling; Hsu, Ching-Hsiang; Hong, Gary
PA United Microelectronics Corporation, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5885868	A	19990323	US 1997-789202	19970124
	TW 428319	B	20010401	TW 1996-85106473	19960531
PRAI	TW 1996-85106473	A	19960531		

AB A process for fabricating compact contactless **flash memory** array for semiconductor EEPROM devices having a no. of memory cell units is disclosed. Field **oxide layers** for the **flash memory** array are 1st grown over the surface of an SOI wafer. Gate **oxide layers** are then grown. **Floating gates** are then formed by patterning the 1st polysilicon layer. **Source/drain** buried bitlines for the **flash memory** array are formed. A 1st BPSG (borophosphosilicate glass) layer is deposited and then reflown and etched back. An **oxide**-nitride-**oxide layer** is formed. A 2nd polysilicon layer is deposited with in-situ dopants. A WSix layer then forms. Stacked gates for the flash array are formed by patterning into the formed oxide-nitride-oxide, 2nd polysilicon and WSix layers. The stacked gates are then covered with a 2nd BPSG layer. Contact openings for the **source/drain** buried lines are formed. Metal lines leading into the contact openings are then formed for interconnecting the memory cells in the **flash memory** array with peripheral control circuits of the semiconductor EEPROM devices.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 90 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:814774 HCAPLUS
DN 132:43751
TI Fabrication of semiconductor **flash memory** devices having **floating gates**

12/05/2002

IN Chikuchi, Masaru
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11354655	A2	19991224	JP 1998-164944	19980612
	JP 3298509	B2	20020702		
	KR 2000006121	A	20000125	KR 1999-21802	19990611
	CN 1239325	A	19991222	CN 1999-109522	19990612
	US 2002063276	A1	20020530	US 1999-332109	19990614
	US 6429072	B1	20020806		
PRAI	JP 1998-164944	A	19980612		

AB The title fabrication involves forming a dummy pattern on a 1st cond.-type semiconductor substrate, doping with a 2nd cond.-type dopant in the areas across the dummy pattern on the substrate to give a **source** and a **drain**, depositing conductive layers each over the **source** and the **drain**, removing the dummy pattern to expose the substrate, forming an **insulator film** to make a gate insulator and an interlayer insulator as a single piece over the exposed substrate portion and the deposited conductive layers, depositing a conductive **layer** over the gate **insulator** and the interlayer insulator, etching to pattern the conductive layer to give a **floating gate** over the gate and areas extended over the **source** and the **drain** on the gate insulator and the interlayer insulator, forming an isolative **insulator layer** over the entire **floating gate**, and forming a controlling **gate** over the **floating gate** on the isolative **insulator layer**. The dummy pattern may be made from a Si nitride film. The gate insulator may be made from a **silica** film. The **floating gate** may be made from doped polysilicon as a conductor layer. The process provides easy formation of a **flash-memory floating gate** which is extended to areas over the **source** and the **drain** regions.

L59 ANSWER 91 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:177231 HCAPLUS
DN 131:26290
TI Properties of **stacked** dielectric **films** composed of **SiO2**/Si3N4/**SiO2**
AU Santucci, S.; Lozzi, L.; Passacantando, M.; Phani, A. R.; Palumbo, E.; Bracchitta, G.; De Tommasis, R.; Torsi, A.; Alfonsetti, R.; Moccia, G.
CS Dipartimento di Fisica and Unita INFM, Universita dell'Aquila, Via Vetoio 10, L'Aquila, 67010, Italy
SO Journal of Non-Crystalline Solids (1999), 245, 224-231
CODEN: JNCSBJ; ISSN: 0022-3093
PB Elsevier Science B.V.
DT Journal
LA English
AB Dielec. films composed of Si oxide-nitride-oxide (ONO) structure were grown over a polycryst. Si phosphorous-doped substrate. The films with a total thickness of .apprx.30 nm were obtained by two different deposition techniques of the top-oxide layer i.e. thermal oxidn. of the nitride layers and low pressure CVD, while the bottom oxide and the nitride layer were obtained by thermal oxidn. and low pressure CVD, resp. The chem. compn. was measured by XPS Auger parameter technique while the thickness of the deposited layers was detd. by the x-ray reflectivity method and

compared with the measurements performed on TEM cross-section images. The influence of the layer compn. and thickness on the elec. properties of the whole film, used as dielec. layer of a capacitor with doped polycryst. Si as electrodes, were studied by measuring current as a function of voltage to study the mechanisms which contribute to an increase of the leakage current with increasing applied voltage. Also, elec. erasable programmable read-only **flash memory** devices built using these dielec. layers in the floating gate structure were measured for 'data retention loss' after thermal stress. The results give a complete picture on the role of the two topmost layers of the ONO structure towards the elec. behavior.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 92 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:12260 HCAPLUS
DN 130:74816
TI Fabrication of a multilevel logic **flash memory** cell
IN Lin, Ruei-ling; Hsu, Ching-hsiang; Liang, Mong-song
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5851881	A	19981222	US 1997-944500	19971006
	US 6166410	A	20001226	US 1998-166390	19981005
PRAI	US 1997-944500	A3	19971006		

AB The invention provides a method of manufg. a split-gate MONOS (metal oxide nitride oxide semiconductor) multilevel logic memory device. The memory device has a poly **stacked** gate transistor in series with a MONOS transistor. The device has a novel operation to achieve multilevel memory storage (e.g., 4 voltage states). The method begins by forming a **tunnel oxide layer** on the surface of a semiconductor substrate. The substrate has a **stacked** gate channel area and a MONOS channel area in the active regions. A poly **floating gate** electrode is formed over the **stacked** gate channel region. An ONO layer having a memory nitride layer is formed over the **floating gate** and the **tunnel oxide layer** over the MONOS channel region. A control gate electrode is formed over the ONO layer spanning across the poly **floating gate** electrode and the MONOS channel region. **Source/drain** regions are formed in the substrate. A poly flash transistor and a MONOS flash transistor combine to form the 4-level logic memory cell of the invention.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 93 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:790342 HCAPLUS
DN 130:46257
TI **Flash memory** device
IN Kim, Keon-soo; Choi, Yong-bae; Yoo, Jong-weon
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 42 pp., Cont.-in-part of U.S. Ser. No. 685,458.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5844270	A	19981201	US 1996-763941	19961212
	JP 09307083	A2	19971128	JP 1996-151350	19960612
	US 5977584	A	19991102	US 1996-685458	19960719
PRAI	KR 1996-16737		19960517		
	US 1996-685458		19960719		
	KR 1995-21401		19950720		

AB A highly integrated **flash memory** device having a stable cell is provided. The device includes a semiconductor substrate of a 1st cond. type; a field **insulating layer** buried in a 1st trench formed in the semiconductor substrate to define an active region; a tunnel **insulating film** formed on the active region; a 1st conductive layer for a **floating gate** formed on the tunnel **insulating film**; spacers formed on both the tunnel **insulating film** and the sidewalls of the 1st conductive **layer**; a buried **insulating layer** buried in a 2nd trench formed by etching the substrate adjacent to the spacers; a buried junction layer contacting a lower portion and sidewalls of the buried **insulating layer**, and acting as a **source** and **drain** region including impurities of a 2nd cond. type; a 2nd conductive layer formed on and connected to the 1st conductive layer to be used as a **floating gate**; an **insulating layer** formed on the 2nd conductive layer; and a 3rd conductive layer for a control gate formed on the **insulating layer**. Accordingly, the **flash memory** device has a cell capable of maintaining stable operation and is appropriate for high integration.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 94 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:564242 HCAPLUS
DN 129:183080
TI SOI compact contactless **flash memory** cell
IN Lin, Ruei-ling; Hsu, Ching-hsiang; Hong, Gary
PA United Microelectronics Corp., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5796142	A	19980818	US 1997-786908	19970122
	TW 428319	B	20010401	TW 1996-85106473	19960531
PRAI	TW 1996-85106473	A	19960531		

AB A compact contactless **flash memory** array for semiconductor EEPROM devices having a no. of memory cell units is described. Field **oxide layers** for the **flash memory** array are 1st grown over the surface of an SOI wafer. Gate **oxide layers** are then grown. **Floating gates** are then formed by patterning a 1st polysilicon layer. **Source/drain** buried bit lines for the **flash memory** array are formed. A 1st BPSG (borophosphosilicate glass) layer is deposited and then reflowed and etched back. An ONO layer is formed. A 2nd polysilicon layer is deposited with in-situ doping. A WSix layer then forms. Stacked gates for the flash array are formed by patterning into the formed oxide-nitride-oxide, 2nd polysilicon, and WSix layers. The stacked gates are then covered with a 2nd BPSG layer. Contact openings for the **source/drain** buried lines are

formed. Metal lines leading into the contact openings are then formed for interconnecting the memory cells in the **flash memory** array with peripheral control circuits of the semiconductor EEPROM devices.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 95 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:98036 HCAPLUS
DN 128:148488
TI Manufacture of a multilevel, split-gate, **flash memory** cell
IN Liang, Mong-Song; Kuo, Di-Son; Hsu, Ching-Hsiang; Lin, Ruei-Ling
PA Taiwan Semiconductor Manufacturing Company, Ltd, Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5714412	A	19980203	US 1996-755868	19961202
	US 5877523	A	19990302	US 1997-974459	19971120
	US 6281545	B1	20010828	US 1998-199130	19981124
PRAI	US 1996-755868	A3	19961202		
	US 1997-974459	A1	19971120		

AB A semiconductor memory device is formed on a doped semiconductor substrate, and covered with a **tunnel oxide layer** covered in turn with a doped 1st polysilicon layer. The 1st polysilicon layer is patterned into a pair of **floating gate** electrodes. An interelectrode **dielec. layer** covers the **floating gate** electrodes, the sidewalls of the **floating gate** electrodes, and the edges of the **tunnel** oxide below the **floating gate** electrodes. A 2nd polysilicon **layer** overlies the interelectrode **dielec. layer** and is in turn covered by a W silicide layer. A 2nd **dielec. layer** covers the W silicide layer. A control gate electrode which spans the pair of **floating gate** electrodes is formed by the 2nd polysilicon layer, the W silicide, and the 1st and 2nd **dielec. layers** patterned into a gate electrode **stack**, providing a control gate electrode spanning across the pair of **floating gate** electrodes. There are **source/drain** regions in the substrate self-aligned with the control gate electrode.

L59 ANSWER 96 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:490453 HCAPLUS
DN 129:183027
TI Stacked floating gate memory device
IN Clemens, James Theodore; Lee, Woo Hyong; Manchanda, Lalita
PA Lucent Technologies Inc., USA
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10189921	A2	19980721	JP 1997-277485	19971009
PRAI	US 1996-27612P	P	19961010		
	US 1996-871024	A	19961010		

AB The invention relates to a stacked floating gate memory device, i.e., **flash memory**, e.g., EPROM, wherein the IPD (inter-poly dielec.) layer interposed between the floating and control gates enables a erasing voltage .gtoreq. 5 V.

L59 ANSWER 97 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:220983 HCAPLUS
DN 128:289074
TI Memory cell array
IN Chiang, Ho Chul; Kim, Jong Goh
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10093057	A2	19980410	JP 1997-233490	19970829
	JP 2960377	B2	19991006		
PRAI	KR 1996-36631		19960830		

AB The invention relates to a stack-gate **flash memory** cell array, wherein the layout enables four memory cells to share a single **drain** and a single **source**, so that the **floating gate** and the field **oxide film** is proportionally enlarged.

L59 ANSWER 98 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:199632 HCAPLUS
DN 128:289033
TI Semiconductor integrated circuits for AND-type nonvolatile **flash memory** devices and fabrication thereof
IN Okazaki, Tsutomu
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 15 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10084052	A2	19980331	JP 1996-237806	19960909

AB The title fabrication involves forming a 1st polycryst. Si film for a **floating gate** lower electrode on a semiconductor substrate, doping the substrate over the Si film as a mask to give a **drain** and a **source**, selectively thermal oxidizing over the **drain** and **source** to give a selective **oxide film**, forming a 2nd polycryst. Si sidewall with a PAD **oxide film** and a polycryst. Si film, forming a 3rd polycryst. Si film for a **floating gate** upper electrode, etching the 3rd polycryst. Si **film** and the selective **oxide film** together with the Si substrate over a single mask to give a trench isolation, and giving a Si **oxide** buried **layer** in the trench for a component isolation structure. The fabrication arrangement provides the memory devices an evenly formed thickness in the selective **oxide film** and an simplified fabrication.

L59 ANSWER 99 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:689521 HCAPLUS
DN 127:354327

TI Making a raised-bitline contactless **trenched flash memory** cell
IN Lin, Ruei-ling; Hsu, Ching-hsiang; Liang, Mong-song
PA Taiwan Semiconductor Manufacturing Company, Ltd, Taiwan
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5679591	A	19971021	US 1996-766079	19961216
	US 5834806	A	19981110	US 1997-873833	19970612
PRAI	US 1996-766079		19961216		

AB A raised-bitline, contactless **flash memory** device with **trenches** on a semiconductor substrate doped to a 1st cond. type includes a 1st well of the opposite cond. type comprising a deep conductor line to a device, and a 2nd well of the 1st cond. type above the 1st well comprising a body line to the device. Deep **trenches** extend through the 2nd well into the 1st well. The **trenches** are filled with a 1st dielec. There are gate electrode **stacks** for a **flash memory** device including a gate **oxide layer** over the device. First doped polysilicon **floating gates** are formed over the gate **oxide layer**. An interpolysilicon **dielec. layer** is formed over the **floating gate** electrodes, and control gate electrodes made of doped polysilicon overlie the interpolysilicon **dielec. layer**. A dielec. cap overlies the control gate electrodes. **Source/drain** regions are formed in the 2nd well self-aligned with the **stacks** as well as spacer dielec. structures formed adjacent to the sidewalls of the **stacks**. A 3rd doped polysilicon layer patterned into raised bit lines overlies the **source/drain** regions.

L59 ANSWER 100 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:344836 HCAPLUS
DN 127:43297
TI Manufacture of **flash memory** devices having metallic **source** lines and self-aligned contacts
IN Sung, Hung-cheng; Chen, Ling
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5631179	A	19970520	US 1995-511062	19950803
	US 5814862	A	19980929	US 1997-801659	19970218
PRAI	US 1995-511062		19950803		

AB Manuf. of an integrated circuit **flash memory** device includes covering a semiconductor substrate with a tunnel **oxide layer**, a **floating gate layer**, an intergate **dielec. layer**, a control gate **layer**, and a **SiO2 dielec. layer** over a Si nitride layer. Then those **layers** over the tunnel **oxide** are patterned into a **flash memory** gate electrode by etching through a **source/drain** mask followed by ion implanting **source/drain** dopant ions through the openings formed by etching. Sidewall spacers are formed, followed by a

dielec. layer through which **source** line openings are etched down to the **source/drain** regions. Plug openings are made down to the **source/drain** regions. An intermetal **dielec. layer** comprising plasma-enhanced **oxide** (PEOX)/SOG/PEOX is deposited over the device. Then via openings are made over the **drain** plugs by etching the intermetal **dielec. layer** through a via mask. Next metal is deposited over the intermetal **dielec. layer** into the via openings extending down into contact with the **drain** plugs.

L59 ANSWER 101 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:321059 HCAPLUS
DN 127:27694
TI Surface treatment of substrate and manufacture of dielectric oxide film with low leak current
IN Izawa, Masaru; Fujisaki, Yoshihisa; Ushiyama, Masahiro; Matsui, Yuichi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09082674	A2	19970328	JP 1995-241293	19950920

AB A Si single crystal substrate is treated with (A) .gtoreq.1 B compd., (B) .gtoreq.1 P halide, or (C) .gtoreq.1 thionyl halide for removal of impurities. The film is manufd. after washing a Si substrate with .gtoreq.1 org. alc. or a NH4OH soln. and treating the substrate surface by the above method. In manuf. of the film by MOCVD, a C compd. is removed by treating the substrate surface with .gtoreq.1 reducing gas. The dielec. film is useful as gate insulating films of transistors, tunnel insulating films of **flash memory** devices, etc. An obtained **Ta2O5** film showed low leak current and good hot-electron resistance.

L59 ANSWER 102 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:148356 HCAPLUS
DN 126:231824
TI Miniaturization of aluminum single-electron devices
AU Tsai, Jaw Shen; Nakamura, Yasunobu; Chen, Chii Dong
CS Fundam. Res. Lab., NEC, Tsukuba, 305, Japan
SO Oyo Butsuri (1997), 66(2), 141-145
CODEN: OYBSA9; ISSN: 0369-8009
PB Oyo Butsuri Gakkai
DT Journal; General Review
LA Japanese
AB A review, with 20 refs., on the principle and possibilities of Al single-electron devices, together with the authors' expt. to give the device with 20 nm islands by electron-beam lithog. The electrochem. microfabrication process to enhance the operating temp. of the device if also discussed. A room-temp. single-electron **flash memory** employing those fabrication methods is proposed.

L59 ANSWER 103 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:722509 HCAPLUS
DN 126:25639
TI Fabrication process for **flash memory** in which channel lengths are controlled
IN Hong, Gary

PA United Microelectronics Corp., Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5576232	A	19961119	US 1994-353673	19941212

AB A process for fabricating memory cells for split-gate **flash memory** devices is disclosed to feature self-alignment and therefore precisely defined channel lengths for the **floating-gate** and isolation transistors of the memory cell. A gate **oxide layer**, a 1st conducting **layer**, and a gate **dielec. layer** are formed in sequence on a semiconductor substrate. A conducting strip is formed on the gate **dielec. layer**. The conducting strip is covered with a shielding layer. The gate **dielec. layer**, the 1st conducting **layer**, and the gate **oxide layer** are etched using the shielding layer as a shielding mask to form a control gate for the memory cell. Thermal oxidn. is applied to the entire substrate using the shielding layer as a shielding mask to form a tunnel **oxide layer** on the surface of the substrate and isolating **oxide layers** on the sidewalls of the control gate. The shielding layer is removed. Elec. conducting sidewall spacers are formed on both of the sidewalls of the conducting strip. Each of the conducting sidewall spacers covers a portion of the tunnel **oxide layer** and is also elec. isolated from the control gate by the isolating **oxide layer**, forming the **floating gate** for the memory cell. Impurities are implanted using the conducting strip and the conducting sidewall spacers as shielding masks to form **source** and **drain** regions on the substrate for the memory cell.

L59 ANSWER 104 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:518771 HCAPLUS
DN 133:98116
TI **Flash memory** and method of manufacturing the same
IN Ahn, Byung-jin
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korea, No pp. given
CODEN: KRXXFC
DT Patent
LA Korean
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 9615936	B1	19961123	KR 1993-16594	19930825

AB The **flash memory** comprises: a gate **oxide film** formed on a p-type semiconductor substrate; a **floating gate** formed on the gate **oxide film** in the shape of a spacer; a selecting channel formed on the substrate of the side wall of the **floating gate** with a p-type impurity; a **source** on the semiconductor substrate neighboring on the selecting channel with an n-type impurity; a **drain** formed on the opposite side to the **source** with an n-type impurity; and an interfacial **oxide film** deposited on the surface of the **floating gate**, and a control gate formed on the gate and the interfacial **oxide films**.

L59 ANSWER 105 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:151340 HCAPLUS
DN 126:165241
TI Fabrication of non-volatile **flash memory** devices for uniform erasing rate
IN Yamauchi, Takahiko
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08330452	A2	19961213	JP 1995-133078	19950531

AB The title fabrication involves forming a gate **insulator film** in a component region which is bound between component isolation regions in a 1st cond.-type semiconductor substrate, forming pl. no. of parallel gate wires across width direction of the components region, and doping the substrate with a 2nd cond.-type dopant over the gate wires as its masks in alignment to the cross-over width on the **source** region side to give **source/drain** regions. The arrangement gives amt. of electron discharged from **floating gate** to **source** region equiv. rate among the cells for uniformed flash erasing time between cells.

L59 ANSWER 106 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:506076 HCAPLUS
DN 125:155981
TI Non-volatile memory and method for manufacturing the same
IN Matsushita, Tadashi
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 53 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 718895	A2	19960626	EP 1995-302992	19950502
	EP 718895	A3	19970326		
	EP 718895	B1	20000927		
	R: DE, FR, GB, NL				
	JP 08227944	A2	19960903	JP 1995-107477	19950501
	JP 3274785	B2	20020415		
	JP 2002151609	A2	20020524	JP 2001-290442	19950501
PRAI	JP 1994-317107	A	19941220		
	JP 1995-107477	A3	19950501		

AB A **flash memory** which comprises: a semiconductor substrate of a first conductive type, a **source** and **drain** impurity diffusion regions of a second conductive type, a channel region formed between the **source** and **drain** impurity diffusion regions, a gate **insulating film** formed on the channel region, a **floating gate** electrode formed on the gate **insulating film**, and a control gate electrode formed at least partially overlapped with the **floating gate** electrode through the intermediary of an **insulating** interlayer **film**, in which the **source** and **drain** impurity diffusion regions are formed with a const. distance in a main surface of the semiconductor substrate and at least a part of the either region is formed in a surface having a crystal face orientation different from the

main surface of the substrate; the channel region is in contact with the **drain** impurity diffusion region and has an inclined region of which surface has a crystal face orientation different from the main surface of the semiconductor substrate; and the **source** impurity diffusion region is placed relatively upper than the **drain** impurity diffusion region.

L59 ANSWER 107 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:94318 HCAPLUS
DN 124:190619
TI Pt/PZT/n-SrTiO3 ferroelectric memory diode
AU Gotoh, Kohtaroh; Tamura, Hirotaka; Takauchi, Hideki; Yoshida, Akira
CS Fujitsu Lab. Ltd., Atsugi, 243-01, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1996), 35(1A), 39-43
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB We fabricated a new nonvolatile ferroelec. memory, which consists of vertical metal-ferroelec.-semiconductor diodes. Our diode has a simpler structure than an Ferroelec. Random Access Memory (FRAM) cell, and operates at a lower voltage than Metal Ferroelec. Semiconductor Field Effect Transistors (MFS-FETs) or conventional **flash memories**. We demonstrated the memory operation using a Pt/PZT/n-SrTiO3 diode in this work. We deposited (001)-oriented PZT on (100) 0.5 wt% Nb doped n-type SrTiO3 substrate using a laser ablation technique. The diodes had a hysteresis loop in their capacitance-voltage characteristics due to ferroelec. polarization in the PZT layer. Their current-voltage curves were Schottky-diode-like and also had a hysteresis loop due to the ferroelec. remanent polarization. We confirmed correct nonvolatile and nondestructive memory readout operation. The write voltages were -5 V to write a logic "0" and above 2.5 V to write a logic "1". The read voltage was 0.8 V.

L59 ANSWER 108 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:958493 HCAPLUS
DN 124:19836
TI Manufacture of a high-density flash EPROM cell
IN Hong, Gary
PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5460988	A	19951024	US 1994-231811	19940425
	US 5721442	A	19980224	US 1997-847876	19970428
PRAI	US 1994-231811		19940425		
	US 1995-499742		19950707		

AB A method for manufg. a high-d. EPROM or **flash memory** cell is described. A structure having Si islands is formed from a device well that has been implanted with a 1st- cond.-type-imparting dopant, over a Si substrate. A 1st **dielec. layer** surrounds the vertical surfaces of the Si islands, whereby the 1st **dielec. layer** is a gate **oxide**. A 1st conductive layer is formed over vertical surfaces of the 1st **dielec. layer**, and acts as the **floating** surrounding-**gate** for the memory cell. A **source** region is formed in the device well by

implanting with a 2nd cond.-type-imparting dopant, and surrounds the base of the Si islands. A **drain** region is in the top of the Si islands, formed by implanting with a 2nd cond.-type-imparting dopant. A thin **dielec. layer** surrounds the Si islands, over the **source** region and under the 1st conductive layer, and acts as a tunnel oxide for the memory cell. A 2nd **dielec. layer** is formed over the vertical surfaces of the 1st conductive layer, and horizontally over the **source** region, and is an interpoly dielec. A 2nd conductive layer is formed over the vertical surfaces of the 2nd **dielec. layer**, and is the control gate for the memory cell.

L59 ANSWER 109 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:739018 HCAPLUS
DN 123:215661
TI Forming a **flash memory** with high coupling ratio
IN Hong, Gary
PA United Microelectronics Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5432112	A	19950711	US 1994-238873	19940506
	US 5675162	A	19971007	US 1996-641411	19960430
PRAI	US 1994-238873		19940506		
	US 1995-445934		19950522		

AB In forming a **flash memory** device on a semiconductor substrate having a **source**, a **drain**, a **dielec. layer** deposited on the substrate, and a 1st **floating gate** electrode formed on the **dielec. layer**, a 2nd **floating gate** electrode is formed on the 1st **floating gate** electrode, a 2nd **dielec. layer** is deposited on the 1st and 2nd **floating gate** electrodes, and a control gate electrode is deposited on the 2nd **dielec. layer**, and means for applying a voltage to the control gate electrode. A Si3N4 layer is formed on the 1st **floating gate** electrode and patterned to form an opening to alloy the 2nd **floating gate** electrode to be deposited on the 1st **floating gate** electrode.

L59 ANSWER 110 OF 110 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:602479 HCAPLUS
DN 123:100135
TI High-density split-gate memory cell for EPROM or **flash memory** and its manufacture
IN Hong, Gary
PA United Microelectronics Corp., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5414287	A	19950509	US 1994-231812	19940425

AB A method and structure for manufg. a high-d. split-gate memory cell are described. Si islands are formed from a Si substrate implanted with a 1st cond.-imparting dopant. A 1st **dielec. layer** surrounds

the vertical surfaces of the Si islands, whereby the 1st **dielec**. **layer** is a gate **oxide**. A 1st conductive layer is formed over a portion of the vertical surfaces of the 1st **dielec**. **layer**, and acts as a **floating gate** for the memory cell. A **source** region is located in the Si substrate, and is implanted with a 2nd and opposite cond.-imparting dopant to the 1st cond.-imparting dopant, and surrounds the base of the Si islands. A **drain** region is located in the top of the Si islands, and is also implanted with a 2nd and opposite cond.-imparting dopant to the 1st cond.-imparting dopant. A 2nd **dielec**. **layer** is formed over the top and side surfaces of the **floating gate**, and acts as an interpoly dielec. A 2nd conductive layer is formed over that remaining portion of the vertical surfaces of the 1st **dielec** . **layer** not covered by the 1st conductive layer, and surrounds the 2nd **dielec**. **layer**, whereby the 2nd conductive layer is a control gate.

L68 ANSWER 1 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-711575 [77] WPIX
DNN N2002-561147 DNC C2002-201911
TI Non-volatile semiconductor memory device, e.g. **flash memory**, has tunnel oxide layer of preset thickness and comprising fluorine atoms.
DC L03 U11 U14
IN NG, C; SHIRAIWA, H; WU, Y; YANG, J Y
PA (ADMI) ADVANCED MICRO DEVICES INC; (FUIT) FUJITSU LTD
CYC 1
PI US 6445030 B1 20020903 (200277)* 10p
ADT US 6445030 B1 US 2001-772600 20010130
PRAI US 2001-772600 20010130
AB US 6445030 B UPAB: 20021129
NOVELTY - Each silicon oxide nitride oxide silicon (SONOS) type memory cell (64) comprises a tunnel oxide layer (54) of thickness from ca. 40 Angstrom to ca. 250 Angstrom and having fluorine atoms. A charge trapping dielectric layer (56) is formed over the tunnel oxide layer and an electrode (58) is formed over the charge trapping dielectric layer. Source and drain regions (60, 62) are formed within a silicon substrate (52).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the production of a SONOS-type non-volatile semiconductor memory cell.
USE - Non-volatile semiconductor memory device, e.g. **flash memory**, read only memory (ROM), programmable read only memory (PROM), erasable programmable read only memory (EPROM) and electrically erasable programmable read only memory (EEPROM).
ADVANTAGE - Since fluorine atoms are present in the tunnel oxide layer, the negative charges are produced in the tunnel oxide layer which renders the tunnel oxide more conductive and increases erase speed or maintains speed consistent over number of program-erase cycles.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the non-volatile semiconductor memory cell.
Silicon substrate 52
Tunnel oxide layer 54
Charge trapping dielectric layer 56
Electrode 58
Source and drain regions 60,62
SONOS-type memory cell 64
Dwg.7/7

L68 ANSWER 2 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-697384 [75] WPIX
DNN N2002-549852 DNC C2002-197449
TI Formation of gate dielectric layer in nitride read only memory for increasing gate controllability, involves forming **zirconium oxide** layer on substrate by sputtering method at preset temperature.
DC L03 U11 U13 U14
IN CHANG, K K
PA (CHAN-I) CHANG K K
CYC 1
PI US 2002086548 A1 20020704 (200275)* 7p
ADT US 2002086548 A1 US 2000-735894 20001214
PRAI US 2000-735894 20001214
AB US2002086548 A UPAB: 20021120
NOVELTY - A method for forming a gate dielectric layer in nitride read only memory (NROM) involves forming a **zirconium oxide** layer (20) on a substrate (10) by sputtering method between 200-800 deg. C.
USE - For forming a gate dielectric layer in NROM.

ADVANTAGE - The method enables the formation of a gate dielectric layer in NROM having excellent gate controllability and ON and OFF characteristics. High dielectric constant **zirconium oxide** layer formed on the substrate reduces control voltage and leakage current, increases current drivability and drain current, exhibits low sub-threshold swing, and improves sub-threshold characteristics and electron and hole mobility. High coupling ratio of gate dielectric layer is increased. Defect density of memory cell is reduced and the reliability of **flash memory** device can be improved.
Zirconium oxide layer is formed on the substrate at lower temperature than conventional thermal oxidation such that thermal budget can be reduced.
DESCRIPTION OF DRAWING(S) - The figure is a schematic representation of gate dielectric layer in NROM.
Substrate 10
Zirconium oxide layer 20
Dwg.5/5

L68 ANSWER 3 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-665452 [71] WPIX
CR 2002-665447 [71]; 2002-665451 [71]
DNN N2002-526434 DNC C2002-186864
TI Formation of silicon-doped **aluminum oxide** for production of transistor, involves co-evaporating **aluminum oxide** and silicon monoxide, and depositing evaporated oxides on substrate to form silicon-doped **aluminum oxide**.
DC L03 U11 U13
IN AHN, K Y; FORBES, L
PA (AHNK-I) AHN K Y; (FORB-I) FORBES L
CYC 1
PI US 2002086556 A1 20020704 (200271)* 11p
ADT US 2002086556 A1 Div ex US 2001-754926 20010104, US 2001-12677 20011105
PRAI US 2001-754926 20010104; US 2001-12677 20011105
AB US2002086556 A UPAB: 20021105
NOVELTY - An **aluminum oxide** and silicon monoxide or co-evaporated, and at least some of evaporated **aluminum oxide** and silicon monoxide are deposited on a substrate (62) to form silicon-doped **aluminum oxide** on the substrate.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) the production of a transistor; and
(2) the formation of a memory device.
USE - For forming a transistor and memory device (claimed), especially for dielectric materials used in transistor gate structures and **flash memory** device structures.
ADVANTAGE - Silicon-doped **aluminum oxide** films of high reliability with low leakage current and high thermal stability are deposited.
DESCRIPTION OF DRAWING(S) - The figure shows the diagrammatic cross-sectional view of semiconductor substrate wafer fragment illustrating **flash memory** device.
Substrate 62
Dwg.8/9

L68 ANSWER 4 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-665451 [71] WPIX
CR 2002-665447 [71]; 2002-665452 [71]
DNN N2002-526433 DNC C2002-186863
TI Formation of silicon-doped **aluminum oxide** used as gate dielectric for transistor and memory device, involves co-evaporating **aluminum oxide** and silicon monoxide, and depositing

vapors on substrate.
DC L03 U11 U13
IN AHN, K Y; FORBES, L
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 2002086555 A1 20020704 (200271)* 11p
ADT US 2002086555 A1 Div ex US 2001-754926 20010104, US 2001-12619 20011105
PRAI US 2001-754926 20010104; US 2001-12619 20011105
AB US2002086555 A UPAB: 20021105
NOVELTY - **Aluminum oxide** and silicon monoxide are co-evaporated. At least some of the evaporated **aluminum oxide** and silicon monoxide are deposited on the substrate to form silicon-doped **aluminum oxide**.
DETAILED DESCRIPTION - The **aluminum oxide** is evaporated from single crystal **sapphire**. The substrate comprises a semiconductor material or monocrystalline silicon.
INDEPENDENT CLAIMS are also included for the following:
(1) the formation of a transistor; and
(2) the formation of a memory device.
USE - Used as a gate dielectric for various semiconductor devices such as transistors, **flash memory** devices (claimed), and metal oxide semiconductor devices.
ADVANTAGE - The process enables the deposition of highly reliable silicon-doped **aluminum oxide** films having low leakage and high thermal stability. The silicon monoxide can be easily evaporated from a thermal source and deposited on a cold substrate with good adhesion. The evaporation source used is relatively cheap, simple and easier to control.
DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of a semiconductor substrate wafer fragment illustrating a **flash memory** device.
Dwg.8/9

L68 ANSWER 5 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-665447 [71] WPIX
CR 2002-665451 [71]; 2002-665452 [71]
DNN N2002-526429 DNC C2002-186859
TI Silicon-doped **aluminum oxide** formation involves co-evaporating and depositing **aluminum oxide** and silicon monoxide on substrate to form silicon-doped **aluminum oxide** layer on substrate.
DC L03 U11 U12
IN AHN, K Y; FORBES, L
PA (AHNK-I) AHN K Y; (FORB-I) FORBES L
CYC 1
PI US 2002086521 A1 20020704 (200271)* 11p
ADT US 2002086521 A1 US 2001-754926 20010104
PRAI US 2001-754926 20010104
AB US2002086521 A UPAB: 20021105
NOVELTY - **Aluminum oxide** and silicon monoxide are co-evaporated and deposited on the substrate (12) provided in the chamber to form the silicon-doped **aluminum oxide** layer on the substrate.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) the production of a transistor; and
(2) the production of memory devices.
USE - For forming a gate in the gate structure of a transistor, e.g. a MOSFET, a **flash memory** or a dynamic random access memory.
ADVANTAGE - Since the aluminum monoxide and silicon monoxide are

deposited on the substrate after evaporation, the protective properties against corrosive agent such as water and hydrogen sulfide is improved. Silicon monoxide films formed by evaporation have attractive optical, electrical and mechanical properties.

DESCRIPTION OF DRAWING(S) - The figures show a cross-sectional view and another view of semiconductor wafer fragment arrangement.
Substrate 12
Dwg.4, 6/9

L68 ANSWER 6 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-518726 [55] WPIX
DNN N2002-410609 DNC C2002-146678
TI Non-volatile semiconductor memory, e.g. SONOS-type **flash memory**, has wordlines and bitlines provided respectively above and below charge trapping dielectric in planar core region.
DC L03 U12
IN DERHACOBIAN, N; RAMSBEY, M T; ROGERS, D M; SHIRAIWA, H; SUNKAVALLI, R S; VAN BUSKIRK, M A; WANG, J S; YANG, J Y; SUNKAVALLI, R; WANG, J; WU, Y
PA (ADMI) ADVANCED MICRO DEVICES INC; (FUIT) FUJITSU LTD; (DERH-I) DERHACOBIAN N; (RAMS-I) RAMSBEY M T; (ROGE-I) ROGERS D M; (SHIR-I) SHIRAIWA H; (SUNK-I) SUNKAVALLI R S; (VBUS-I) VAN BUSKIRK M A; (WANG-I) WANG J S; (YANG-I) YANG J Y
CYC 96
PI US 2002063277 A1 20020530 (200255)* 24p
WO 2002045157 A1 20020606 (200255) EN
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
WO 2002045171 A1 20020606 (200255) EN
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
AU 2001083186 A 20020611 (200264)
AU 2002020164 A 20020611 (200264)
ADT US 2002063277 A1 CIP of US 2000-723635 20001128, US 2001-893026 20010627; WO 2002045157 A1 WO 2001-US24829 20010807; WO 2002045171 A1 WO 2001-US46124 20011115; AU 2001083186 A AU 2001-83186 20010807; AU 2002020164 A AU 2002-20164 20011115
FDT AU 2001083186 A Based on WO 200245157; AU 2002020164 A Based on WO 200245171
PRAI US 2001-893026 20010627; US 2000-723635 20001128
AB US2002063277 A UPAB: 20021031
NOVELTY - Wordlines and buried bitlines are respectively placed above and below a charge trapping dielectric (14) which is provided in the planar core region of a substrate. The periphery region of the substrate has a gate dielectric.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a SONOS-type **flash memory**.

USE - E.g. silicon oxide-nitride-oxide silicon (SONOS)-type **flash memory** (claimed).

ADVANTAGE - Since the core region of the substrate has a planar surface, the need for etching of the core region is avoided, hence high temperature thermal cycling associated with locos formation in the core region is eliminated and thus short channeling effects are minimized.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view

of a non-volatile semiconductor memory.
Charge trapping dielectric 14
Dwg.18/22

L68 ANSWER 7 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-489028 [52] WPIX
CR 2002-016911 [02]; 2002-415214 [44]
DNN N2002-386560 DNC C2002-138840
TI Gate fabrication, for EPROM and EEPROM, involves etching conductive layer formed on dielectric layer using mask layer to form upper portion of floating gate.
DC L03 U11 U13 U14
IN CHANG, C
PA (CHAN-I) CHANG C; (MACR-N) MACRONIX INT CO LTD
CYC 1
PI US 2002052099 A1 20020502 (200252)* 19p
US 6448605 B1 20020910 (200267)
ADT US 2002052099 A1 Cont of US 2000-734406 20001211, US 2001-924904 20010808; US 6448605 B1 Cont of US 2000-734406 20001211, US 2001-924904 20010808
FDT US 2002052099 A1 Cont of US 6300196; US 6448605 B1 Cont of US 6300196
PRAI TW 2000-119796 20000926
AB US2002052099 A UPAB: 20021018
NOVELTY - A conductive layer (116a) having an opening (118) with tapered side wall is formed on the dielectric layer (112). A mask layer (120) is formed to cover the conductive layer. A portion of the mask layer outside the opening is removed leaving the other layer portion in the opening. The conductive layer is etched anisotropically using the mask layer to form upper portion of the floating gate.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a gate structure.
USE - Used for EPROM, EEPROM, DRAM, etc.
ADVANTAGE - As the mask layer itself is used as a mask during etching process, the need for additional photomask is eliminated. Enables reliable fabrication of floating gate having increased surface and tapered inner and outer side walls. As the vertical etching thickness of the dielectric layer between the gates in the non-gate region is reduced, the surface area of the dielectric layer between the gates is increased. Enhances performance of gates and capacitance between the floating gate and control gate.
DESCRIPTION OF DRAWING(S) - The figure shows a section of the non-volatile **flash memory**.
Dielectric layer 112
Conductive layer 116a
Opening 118
Mask layer 120
Dwg.5D/6

L68 ANSWER 8 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-349053 [38] WPIX
TI Method for manufacturing **flash memory** device.
DC U13
IN JU, G C
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2001065670 A 20010711 (200238)* 1p
ADT KR 2001065670 A KR 1999-65590 19991230
PRAI KR 1999-65590 19991230
AB KR2001065670 A UPAB: 20020618
NOVELTY - A method for manufacturing a **flash memory** device is provided to obtain a dielectric layer with a high dielectric constant by repeating efficiently an amorphous **tantalum**

oxide deposition process and a plasma annealing process.

DETAILED DESCRIPTION - A tunnel oxide layer(20) and a floating gate(30) are deposited on a substrate(10). A hemispheric polysilicon layer(50) is deposited on the floating gate(30). The first annealing process is performed. A **tantalum oxide** layer(40) is deposited thereon. The second annealing process is performed. The **tantalum oxide** layer(40) of a predetermined thickness is deposited by repeating the **tantalum oxide** layer deposition process and the second annealing process. The third annealing process is performed. A control gate(60) is deposited thereon.

Dwg.1/10

L68 ANSWER 9 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-257709 [30] WPIX
DNN N2002-199500 DNC C2002-076747
TI Memory cell, used as a non-volatile **flash memory**, comprises a series of layers comprising a storage layer between limiting layers arranged between the source region and the gate electrode and between the drain region and the gate electrode.
DC L03 U11 U13
IN PALM, H; WILLER, J; GRATZ, A; KRIZ, J; ROEHRICH, M
PA (INFN) INFINEON TECHNOLOGIES AG; (PALM-I) PALM H; (WILL-I) WILLER J
CYC 30
PI WO 2002015276 A2 20020221 (200230)* DE 31p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: BR CA CN IL IN JP KR MX RU UA
DE 10039441 A1 20020228 (200230)
US 2002024092 A1 20020228 (200230)
ADT WO 2002015276 A2 WO 2001-DE2997 20010806; DE 10039441 A1 DE 2000-10039441 20000811; US 2002024092 A1 US 2001-900654 20010706
PRAI US 2001-900654 20010706; DE 2000-10039441 20000811
AB WO 200215276 A UPAB: 20020513

NOVELTY - Memory cell comprises a memory transistor having a gate electrode (2) on the upper side of a semiconductor body or a semiconductor layer. The gate electrode is arranged between a source region (3) and a drain region (4) formed in the semiconductor material.

DETAILED DESCRIPTION - A series of layers comprising a storage layer (6) between limiting layers (5, 7) is arranged between the source region and the gate electrode and between the drain region and the gate electrode. INDEPENDENT CLAIMS are also included for:

(a) an arrangement of memory cells; and

(b) a process for the production of a memory cell comprising forming a trench or a number of parallel trenches in a semiconductor body or layer to form doped regions provided as a source, a drain and a bit line, forming a memory medium in the trenches, and applying an electrically conducting material for a gate electrode in the trenches and structuring a conducting pathway as a word line.

Preferably the gate electrode is arranged in a trench formed in the semiconductor material. The limiting layers contain **Al2O3** or **Ta2O5**. The storage layer is **tantalum oxide** or tantalate, hafnium silicate or **hafnium oxide**, **titanium oxide** or titanate, or **zirconium oxide**, **lanthanum oxide** or **aluminum oxide**.

USE - Used as a non-volatile **flash memory**.

ADVANTAGE - The cell has an extremely low space requirement.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the memory cell.

Gate electrode 2
Source region 3
Drain region 4

Limiting layers 5, 7
Storage layer 6
Dwg.3/13

L68 ANSWER 10 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-235351 [29] WPIX
DNN N2002-180678 DNC C2002-071432
TI Floating gate stack for memory cells comprises two polysilicon layers, dielectric layer, barrier layer, metal layer, cap layer, oxidation barrier and sidewall oxide layer.
DC L03 U12
IN PAN, P; PRALL, K D
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6288419 B1 20010911 (200229)* 17p
ADT US 6288419 B1 US 1999-350687 19990709
PRAI US 1999-350687 19990709
AB US 6288419 B UPAB: 20020508
NOVELTY - A floating gate stack comprises a first polysilicon layer (215), a dielectric layer (220), a second polysilicon layer (225), a barrier layer (230), a metal layer (235), a cap layer (240), an oxidation barrier (245) adjacent the sidewalls of the metal layer, and a sidewall oxide layer (250) adjacent the sidewalls of the first polysilicon layer.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(A) a semiconductor die comprising a substrate, and an integrated circuit supported by the substrate and having the inventive floating gate stack(s);

(B) a **flash memory** device comprising an array of floating gate memory cells having the inventive floating gate stack(s), row and column decoder circuits coupled to the memory cells, and an address buffer circuit coupled to the row and column decoder circuits;

(C) a memory module comprising a support, leads extending from the support, command link and data links coupled to the leads, and the **flash memory** device contained on the support and coupled to the command link;

(D) a memory system comprising a controller, command and data links coupled to the controller, and the **flash memory** device coupled to the command and data links; and

(E) an electronic system comprising a processor, and a circuit module having leads coupled to the processor and semiconductor die coupled to the leads.

USE - For floating gate memory cells.

ADVANTAGE - The inventive gate stack has metal control gate which permits reduced gate resistance and gate height over polysilicon or silicide control gates. The oxidation barrier can protect the metal control gate from oxidation during oxidation of sidewalls of the polysilicon-floating gate.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the floating gate stack.

First polysilicon layer 215
Dielectric layer 220
Second polysilicon layer 225
Barrier layer 230
Metal layer 235
Cap layer 240
Oxidation barrier 245
Sidewall oxide layer 250
Dwg.2I/9

L68 ANSWER 11 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-065552 [09] WPIX

DNN N2002-048689 DNC C2002-019340
TI Method of forming **flash memory** cell involves forming **tantalum pentoxide** layer using organic tantalum compound and oxygen compound on oxide layer which is formed on doped polysilicon layer and heating in nitrous oxide.
DC L03 U11 U13 U14
IN AU, K W; CHANG, K K; CHI, D
PA (AUKW-I) AU K W; (CHAN-I) CHANG K K; (CHID-I) CHI D; (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6309927 B1 20011030 (200209)* 10p
US 2001046738 A1 20011129 (200209)
ADT US 6309927 B1 US 1999-263983 19990305; US 2001046738 A1 US 1999-263983 19990305
PRAI US 1999-263983 19990305
AB US 6309927 B UPAB: 20020208
NOVELTY - **Tantalum pentoxide** layer (46b) is formed on oxide layer (46a) which is formed on doped polysilicon layer (44), by chemical vapor deposition (CVD) at 200-650 deg. C using organic tantalum compound and oxygen compound, and heating in nitrous oxide atmosphere at 700-850 deg. C. Another polysilicon layer is formed on the pentoxide layer.
DETAILED DESCRIPTION - The polysilicon layers and the oxide layers (46a, 46b) are etched to form a stacked gate structure.
INDEPENDENT CLAIMS are also included for the following:
(a) a method of forming an insulating layer for a **flash memory** cell; and
(b) a method for forming a high K interpoly dielectric layer
USE - The method is used for forming a **flash memory** cell e.g. flash electrical erasable programmable read only memories (EEPROMs).
ADVANTAGE - Reliability of interpoly dielectric layer is increased in **flash memory** cells by forming a bilayer interpoly dielectric having a high dielectric constant, low defect density and less interface traps. Charge leakage from floating gate to control gate is prevented while Fowler-Nordheim electron tunneling is facilitated.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **flash memory** cell fabrication method.
Substrate 40
Doped polysilicon layer 44
Oxide layers 46a, 46b
Dwg.2C/2

L68 ANSWER 12 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-040559 [05] WPIX
DNN N2002-030041 DNC C2002-011481
TI Magnetic recording medium useful for e.g. video tape recorder, includes magnetic layer(s) comprising binder, lubricant, and ferromagnetic alloy powder.
DC A85 L03 M27 T03
IN HANAI, K; KATO, K; ONO, M
PA (SONY) SONY CORP; (HANA-I) HANAI K; (KATO-I) KATO K; (ONOM-I) ONO M
CYC 2
PI US 2001008713 A1 20010719 (200205)* 11p
JP 2001169232 A 20010622 (200205) 13p
ADT US 2001008713 A1 US 2000-732708 20001211; JP 2001169232 A JP 1999-350455 19991209
PRAI JP 1999-350455 19991209
AB US2001008713 A UPAB: 20020123
NOVELTY - A magnetic recording medium comprises a support, and magnetic layer(s) comprising a binder, lubricant, and ferromagnetic alloy powder

including elemental iron. The magnetic recording medium has surface scratch depth of 370-460 nm, and has a surface lubricant index of 4-11.

USE - Useful for video tape recorder (VTR) or computer devices.

ADVANTAGE - The inventive magnetic recording medium has less abrasion of head and excellent traveling or running property and durability. It has excellent still characteristics, resistance to staining, and superior in signals to noise (C/N) ratio.

Dwg.0/0

L68 ANSWER 13 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2002-016911 [02] WPIX
CR 2002-415214 [44]; 2002-489028 [52]
DNN N2002-013605 DNC C2002-004671
TI Manufacture of gate on substrate by forming conductive layer on dielectric layer and floating gate, patterning conductive layer, forming mask layer, doing anisotropic etching process and removing etching mask layer.
DC L04 U11
IN JANG, C; CHANG, C
PA (MACR-N) MACRONIX INT CO LTD
CYC 2
PI US 6300196 B1 20011009 (200202)* 17p
TW 463248 A 20011111 (200248)
ADT US 6300196 B1 US 2000-734406 20001211; TW 463248 A TW 2000-119796 20000926
PRAI TW 2000-119796 20000926
AB US 6300196 B UPAB: 20020820

NOVELTY - A gate is made on a substrate by forming a first conductive layer on a first dielectric layer and on a lower portion of a floating gate; patterning the first conductive layer; forming a mask layer to cover the conductive layer and fill a second opening; removing the mask layer outside the second opening; performing a first anisotropic etching process; and removing the etching mask layer.

DETAILED DESCRIPTION - Fabrication of a gate over a substrate comprising a first dielectric layer (122) having a first opening, a gate dielectric layer (106) formed in the first opening, a lower portion of a floating gate formed on the gate dielectric layer, and a source/drain region formed in the substrate beside the lower portion of the floating gate, comprises (a) forming a first conductive layer (124) on the first dielectric layer and on the lower portion of the floating gate to completely fill the first opening; (b) patterning the first conductive layer to form a second opening in the first conductive layer, above the first opening but does not expose the first dielectric layer; (c) forming a mask layer to cover the first conductive layer and fill the second opening; (d) removing the mask layer outside the second opening to expose the first conductive layer, where a portion of the mask layer is removed to leave a first etching mask layer in the second opening; (e) performing a first anisotropic etching process using the first etching mask layer as a mask to etch the first conductive layer, where an upper portion of the floating gate is formed, and the first dielectric layer is exposed; and (f) removing the etching mask layer. The second opening has a tapered sidewall and a predetermined depth.

USE - For fabricating a gate over a substrate.

ADVANTAGE - The inventive method increases the effective surface area of the dielectric layer between the gates (a dielectric layer between a floating gate and a control gate), and reduces the vertical etching thickness of the dielectric layer between gates.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the stacked-gate non-volatile **flash memory**.

Gate dielectric layer 106
Dielectric layer 122
Conductive layer 124

Dwg.5H/6

L68 ANSWER 14 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2001-520929 [57] WPIX
CR 2001-079722 [09]
DNN N2001-385856 DNC C2001-155669
TI Manufacture of semiconductor device, e.g. flash electrically erasable programmable read only memories, involves cleaning second oxide dielectric layer to reduce third thickness.
DC L03 U11 U13
IN BUI, N D
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 2001015456 A1 20010823 (200157)* 8p
US 6413820 B1 20020702 (200248)
ADT US 2001015456 A1 Div ex US 1998-170061 19981013, US 2000-725843 20001130; US 6413820 B1 Div ex US 1998-170061 19981013, US 2000-725843 20001130
FDT US 2001015456 A1 Div ex US 6163049; US 6413820 B1 Div ex US 6163049
PRAI US 1998-170061 19981013; US 2000-725843 20001130
AB US2001015456 A UPAB: 20020730
NOVELTY - A semiconductor device is manufactured by cleaning a second oxide dielectric layer to reduce a third thickness to a fourth thickness. The second dielectric layer is deposited on a nitride dielectric layer having the third thickness. A control gate on the second oxide dielectric layer has the fourth thickness.

DETAILED DESCRIPTION - Manufacture of a semiconductor device involves sequentially depositing a first oxide dielectric layer (601) on floating gate (500), a nitride dielectric layer (602) and a second oxide dielectric layer (603) at first to third thickness, respectively. The second oxide dielectric layer is cleaned to reduce the third thickness to a fourth thickness. A control gate (700) on the second oxide dielectric layer has the fourth thickness. The device comprises the floating gate formed on a channel region (300) of a substrate (100) and the control gate above and spaced apart from the floating gate at a distance which corresponds to at least minimum design data retention.

An INDEPENDENT CLAIM is also included for a semiconductor device comprising a tunnel oxide layer (400) on a channel region, a floating gate, a control gate and a composite dielectric layer having first oxide, nitride, and second oxide layers.

USE - For manufacturing semiconductor device, e.g. flash electrically erasable programmable read only memories.

ADVANTAGE - The inventive method solves problems of stemming from thinning of the dielectric layer between the floating and control gates during cleaning, and facilitates cost-effective device. A reduction in the thickness of interpoly dielectric layer adversely affects the performance of the device, e.g. data retention. It increases the difficulty of scaling the device for miniaturization and reduces power consumption.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a **flash memory** cell produced from the inventive method.
Substrate 100
Channel region 300
Tunnel oxide layer 400
Floating gate 500
First oxide dielectric layer 601
Nitride dielectric layer 602
Second oxide dielectric layer 603
Control gate 700
Dwg.2/3

L68 ANSWER 15 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2001-079722 [09] WPIX
CR 2001-520929 [55]

DNN N2001-060677 DNC C2001-022863
TI Non-volatile semiconductor memory device includes second oxide layer with greater thickness and high dielectric constant.
DC L03 U11 U12 U13 U14
IN BUI, N D
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6163049 A 20001219 (200109)* 7p
ADT US 6163049 A US 1998-170061 19981013
PRAI US 1998-170061 19981013
AB US 6163049 A UPAB: 20011010
NOVELTY - A non-volatile semiconductor memory device comprises a composite dielectric layer between a floating gate and a control gate. The dielectric layer has a second oxide layer with a greater thickness and a high dielectric constant.

DETAILED DESCRIPTION - A non-volatile semiconductor memory device comprises a tunnel oxide layer (400) on a channel region (300) of a semiconductor substrate (100), a floating gate (500), a control gate (700) above and spaced apart from the floating gate of at least a distance, and a composite dielectric layer between the floating gate and control gate. The dielectric layer (600) comprises a first oxide layer (601) with a first thickness on the floating gate, a nitride layer (602) with a second thickness, and a second oxide layer (603) with a dielectric constant of at least 10 and a third thickness. The sum of the thicknesses corresponds to at least a minimum design data retention. The oxide layers and nitride layer have a combined capacitance corresponding to the design rule of the device.

USE - As non-volatile semiconductor memory device, e.g. electrically erasable programmable read only memories.

ADVANTAGE - The invention does not reduce the data retention of the **flash memory** device below the design requirements and increases the difficulty of scaling the device for miniaturization and reduction of power consumption. The invention enables widening the cleaning process window without adverse impact on device performance and increases process flexibility.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the device.

Semiconductor substrate 100
Channel region 300
Tunnel oxide layer 400
Floating gate 500
Dielectric layer 600
First oxide layer 601
Nitride layer 602
Second oxide layer 603
Control gate 700
Dwg.2/3

L68 ANSWER 16 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2000-490162 [43] WPIX
DNN N2000-363713 DNC C2000-147167
TI Nonvolatile memories utilize recessed floating gate structure to suppress the short channel effect.
DC L03 U11 U12 U13 U14
IN WU, S
PA (TEXI) TEXAS INSTR ACER INC
CYC 1
PI US 6084265 A 20000704 (200043)* 8p
ADT US 6084265 A US 1998-50540 19980330
PRAI US 1998-50540 19980330
AB US 6084265 A UPAB: 20000907

NOVELTY - Nonvolatile memories comprises field oxides on the semiconductor substrate; buried bit lines beneath field oxides; trenched floating gates between field oxides; tunnel dielectrics between trenched floating gates and substrate; interpoly dielectric on the field oxides and trenched floating gates; and control gates on the interpoly dielectrics.

DETAILED DESCRIPTION - Nonvolatile memories comprises field oxides (12) on the semiconductor substrate (2); buried bit lines (10) beneath the field oxides; trenched floating gates (16) between field oxides; tunnel dielectrics (14) between the trenched floating gates and the substrate; interpoly dielectric (18) on the field oxides and trenched floating gates; and control gates (20) on interpoly dielectrics. The tunnel dielectrics have ends respectively adjacent to one of the buried bit lines, and have recessed geometry conformable with the sidewall and bottom surfaces of the trenched floating gates.

USE - For use as read-only memories (ROM), programmable ROM (PROM), erasable PROM, electrically erasable PROM, and **flash memories**.

ADVANTAGE - The memory has recessed floating gate structure which suppresses the short channel effect and allows the device integration to be increased. It has recessed tunnel having larger area than that of traditional memory structure, giving then faster programming and erasing speeds of the memory as compared to the traditional one.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a semiconductor wafer with recessed floating gate.

Semiconductor substrate 2
Buried bit lines 10
Tunnel dielectrics 14
Trenched floating gates 16
Interpoly dielectric 18
Control gates 20
Dwg.9/10

L68 ANSWER 17 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2000-368605 [32] WPIX
CR 1998-452233 [39]
DNN N2000-275929 DNC C2000-111494
TI Semiconductor device such as MOSFET, DRAM, has metallic oxide of third group or fifth group metal doped with fourth group element so that dopant has preset weight percentage of dielectric material.
DC L03 U11 U12 U13 U14
PA (LUCE) LUCENT TECHNOLOGIES INC
CYC 2
PI JP 11297867 A 19991029 (200032)* 6p
KR 99077767 A 19991025 (200052)
KR 319571 B 20020109 (200253)
ADT JP 11297867 A JP 1999-65742 19990312; KR 99077767 A KR 1999-8028 19990311; KR 319571 B KR 1999-8028 19990311
FDT KR 319571 B Previous Publ. KR 99077767
PRAI US 1998-41434 19980312
AB JP 11297867 A UPAB: 20020823

NOVELTY - The device has a dielectric material formed with a metallic oxide, selected from a group containing **aluminum oxide**, **yttrium oxide**, **tantalum pentoxide** and vanadium oxide, doped with an element selected from the group consisting of zirconium, silicon, titanium and hafnium so that the amount of the dopant in the dielectric material is within 0.1-30 wt%.

USE - For e.g. MOSFET, MISFET, non-volatile memory device such as EPROM, EEPROM, DRAM, **flash memory**.

ADVANTAGE - Prevents leakage of electric charge. Enables to reduce thickness of dielectric layer.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of MOSFET.

Dwg.1/4

L68 ANSWER 18 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2000-328046 [28] WPIX
DNN N2000-246889 DNC C2000-099358
TI Fabrication of a memory device comprises a high performance stacked dielectric sandwiched between two polysilicon plates having a high permittivity layer and two low permittivity buffer layers.
DC L03 U11 U13 U14
IN GARDNER, M I; GILMER, M C; SPIKES, T E
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6048766 A 20000411 (200028)* 8p
ADT US 6048766 A US 1998-172410 19981014
PRAI US 1998-172410 19981014
AB US 6048766 A UPAB: 20000613
NOVELTY - A memory device is fabricated by forming a polysilicon layer over a dielectric stack to have a high performance stacked dielectric sandwiched between two polysilicon plates having a high permittivity layer and two low permittivity buffer layers.
DETAILED DESCRIPTION - Fabrication of memory devices comprising (a) forming a polysilicon plate (202) over a substrate (201); (b) forming a dielectric stack (206) over the plate which includes a high permittivity layer disposed between the buffer layers; (c) forming a second polysilicon plate (204) over the dielectric stack comprising two buffer layers, which are relatively low permittivity layers and another buffer layer, being a relatively high permittivity layer.
USE - For fabricating **flash memory** devices for use in electronics industry.
ADVANTAGE - The method provides a new high performance dielectric layer which increases the speed and reliability of the memory device as compared to the conventional memory devices.
DESCRIPTION OF DRAWING(S) - The figure shows the memory device of the invention.
Substrate 201
Polysilicon plates 202, 204
Dielectric stack 206
Source region 208
Drain region 210
Dwg.2/3

L68 ANSWER 19 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 2000-085507 [07] WPIX
CR 1998-021140 [03]; 1998-021141 [03]; 1998-021272 [03]; 1998-274398 [25]; 1998-274571 [25]; 1998-312838 [27]; 1998-557907 [47]; 1999-132507 [11]; 1999-508244 [42]; 2000-316279 [27]; 2001-023107 [62]; 2001-167538 [62]; 2001-578916 [47]
DNN N2000-067025 DNC C2000-023826
TI Metal-insulator-metal structure formation used during non-volatile memory fabrication.
DC L03 U11 U12 U13 U14
IN WU, S
PA (WUSS-I) WU S
CYC 1
PI US 5998264 A 19991207 (200007)* 9p
ADT US 5998264 A CIP of US 1998-36027 19980306, US 1999-266552 19990311
PRAI US 1999-266552 19990311; US 1998-36027 19980306
AB US 5998264 A UPAB: 20011220
NOVELTY - A conductive layer (30) serving as floating gate is formed over the polished polysilicon layers (8,28). Subsequently, the silicon nitride layer (32) deposited by JVD is formed over the conductive layer. A

dielectric and conductive layer (34,36) are formed sequentially over the nitride layer. The conductive layer (36) serves as control gate.

DETAILED DESCRIPTION - The silicon nitride layer (32) acts as the barrier. The dielectric layer (34) comprises materials selected from **TiO2, Ta2O5, Al2O3,** BSTY2O3 or PZT. The conductive layer (30) comprises the material selected from TiN, WN, TaN or n+ doped silicon. The conductive layer (36) comprises materials selected from TiN, WN, TaN, Ti, W, Pt.

USE - Employed during fabrication of non-volatile memories such as **flash memory** used in computers, portable handy terminal, solid state camera and PC cards.

ADVANTAGE - The electron tunneling efficiency is increased as undoped hemispherical grained silicon or amorphous silica is used to form textured tunneling oxide. As metal-insulator-metal structure is used, the capacitive coupling ratio and the speed of operation of the memory is increased.

DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional view of semiconductor wafer illustrating step of forming multilevel metal structure.

Polysilicon layers 8,28
Conductive layers 30,36
Silicon nitride layer 32

Dwg.9/10

L68 ANSWER 20 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 1999-596875 [51] WPIX
DNN N1999-441152 DNC C1999-174146
TI Formation of floating gate structure for laminated gate programmable IGFET - involves forming dielectric layers of **tantalum oxide** , silicon oxide in-between floating gate and control gate.
DC L03 U11 U12 U13 U14
IN GREGOR, R W; KIZILYALLI, I C; ROY, P K
PA (LUCE) LUCENT TECHNOLOGIES INC
CYC 3
PI JP 11260938 A 19990924 (199951)* 7p
US 6008091 A 19991228 (200007)
KR 99068059 A 19990825 (200046)
KR 284935 B 20010315 (200216)
ADT JP 11260938 A JP 1999-15684 19990125; US 6008091 A US 1998-14030 19980127; KR 99068059 A KR 1999-1861 19990122; KR 284935 B KR 1999-1861 19990122
FDT KR 284935 B Previous Publ. KR 99068059
PRAI US 1998-14030 19980127
AB JP 11260938 A UPAB: 19991207

NOVELTY - The dielectric layer (34) has two SiO2 layers (35), five **Ta2O5** layers (36), and another SiO2 layer (37) with thickness ranging from 10-30 Angstrom , 30-100 Angstrom and 5-30 Angstrom respectively. Thus the overall thickness of dielectric layer ranges from 45-150 Angstrom . The SiO2-**Ta2O5**-SiO2 layers are then annealed at temperature ranging from 550-750 deg. C. DETAILED DESCRIPTION - Dielectric layer (31) is formed on the silicon substrate above which floating gate (32) is formed. The dielectric layer (34) is formed between the floating gate (32) and the control gate (33).

USE - For laminated gate programmable IGFET used in **flash memory**.

ADVANTAGE - Reading and write-in voltage of the IGFET is reduced and the characteristics of floating gate structure is improved. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of memory. (31,34) Dielectric layers; (32) Floating gate; (33) Control gate; (35,37) SiO2 layers; (36) **Ta2O5** layers.

Dwg.1/5

L68 ANSWER 21 OF 22 WPIX (C) 2002 THOMSON DERWENT
AN 1991-372909 [51] WPIX
DNN N1991-285255
TI Control device with reading device for mark on card - decides error when read mark is defectively read, and when information error is present at read mark NoAbstract Dwg 4/9.
DC T01 T04 W05
PA (TOKE) TOSHIBA LIGHTECH KK
CYC 1
PI JP 03250591 A 19911108 (199151)*
ADT JP 03250591 A JP 1990-47451 19900228
PRAI JP 1990-47451 19900228
AB JP 03250591 A UPAB: 19940831
In an electroluminescence (EL) device having a lower electrode on a substrate, an organic multiplex layer contg. a luminescence layer, and a counter-electrode, the EL device has a patterned interlayer insulation film between the lower electrode and the counter electrode.

The inter-layer insulation film pref. consists of inorganic material such as Si oxide, Si nitride or **Al oxide**, or organic material such as polyimide. The inorganic insulation film can be produced by vapour deposition, spattering or plasma CVD, and the organic insulation film can be produced by spin coating, casting or LB method. The patterning of the interlayer insulation film can be effected by a wet or dry etching using a photo-resist. Said substrate of the EL device is e.g. glass, quartz or transparent plastics.

USE/ADVANTAGE - Bright and uniform luminescence can be obtd., and the EL device also shows excellent impact resistance, and can be produced in a simple process. @(10pp Dwg.No.1/2)@

L68 ANSWER 22 OF 22 JAPIO COPYRIGHT 2002 JPO
AN 1995-326681 JAPIO
TI SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE
IN ENDO NOBUHIRO
PA NEC CORP
PI JP 07326681 A 19951212 Heisei
AI JP 1994-116394 (JP06116394 Heisei) 19940530
PRAI JP 1994-116394 19940530
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995
AB PURPOSE: To increase the writing erasing frequency of information electric charge, and obtain a **flash memory** of low voltage or low consumption power, by specifying the relation of thicknesses and specific dielectric constant of a first insulating film and a second insulating film laminated on a semiconductor substrate.
CONSTITUTION: A first insulating film 3 composed of, e.g. silicon oxide, silicon nitride, etc., is formed on the main surface of a semiconductor substrate 1. A second insulating film 4 composed of, e.g. **tantalum pentoxide**, strontium titanate, etc., is laminated on the film 3. The thickness and the specific dielectric constant of the first insulating film 3 are t<SB>1</SB> and ε<SB>1</SB>, respectively. The thickness and the specific dielectric constant of the second insulating film 4 are t<SB>2</SB> and ε<SB>2</SB>, respectively. The relations 20<=ε<SB>2</SB>/ε<SB>1</SB> and t<SB>2</SB>/t<SB>1</SB><=ε<SB>2</SB>/ε<SB>1</SB> are satisfied. Thereby the writing erasing time of information electric charge is reduced, so that the writing erasing frequency is increased, and a **flash memory** of low voltage or low consumption power can be obtained.
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